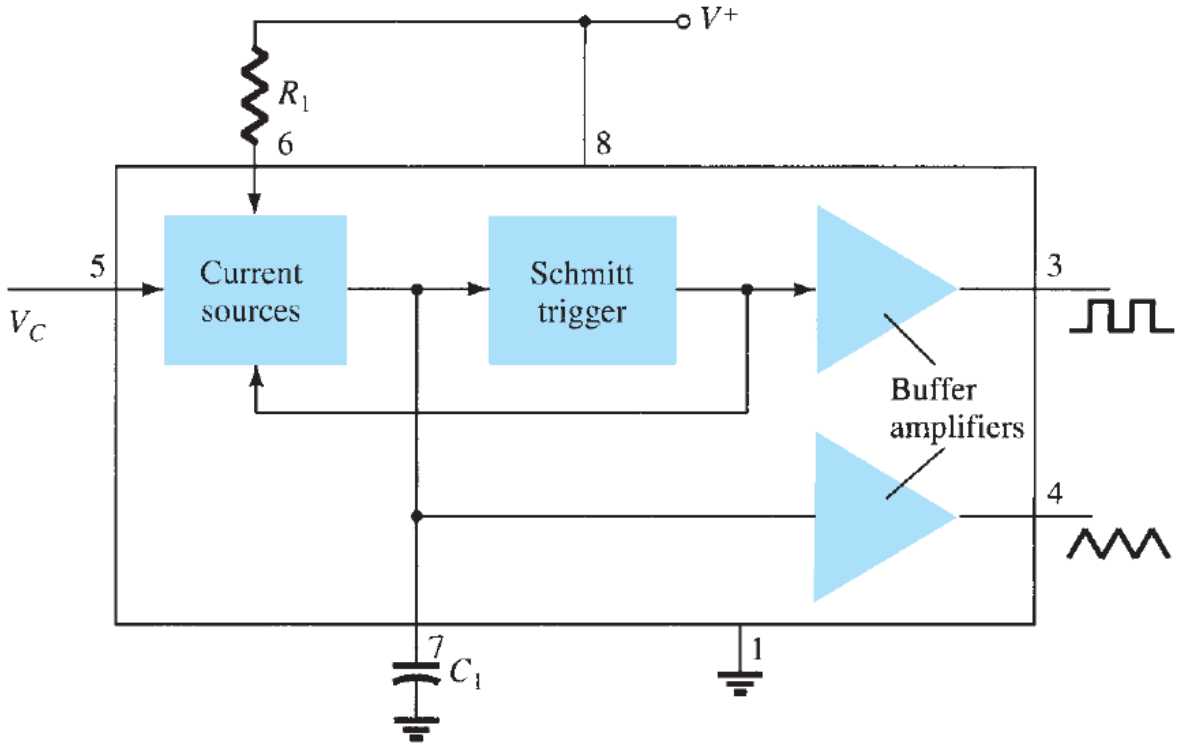
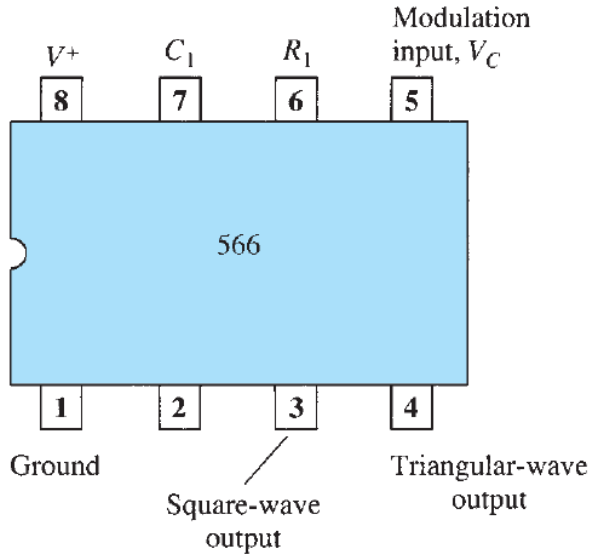
Linear Integrated Circuits

Voltage Controlled Oscillator





- Current sources charge and discharge an external capacitor C_1 at a rate set by external resistor R_1 and the modulating dc input voltage
- Schmitt trigger circuit switches the current sources between charging and discharging the capacitor
- Triangular voltage developed across the capacitor and square wave from the Schmitt trigger are provided as outputs through buffer amplifiers

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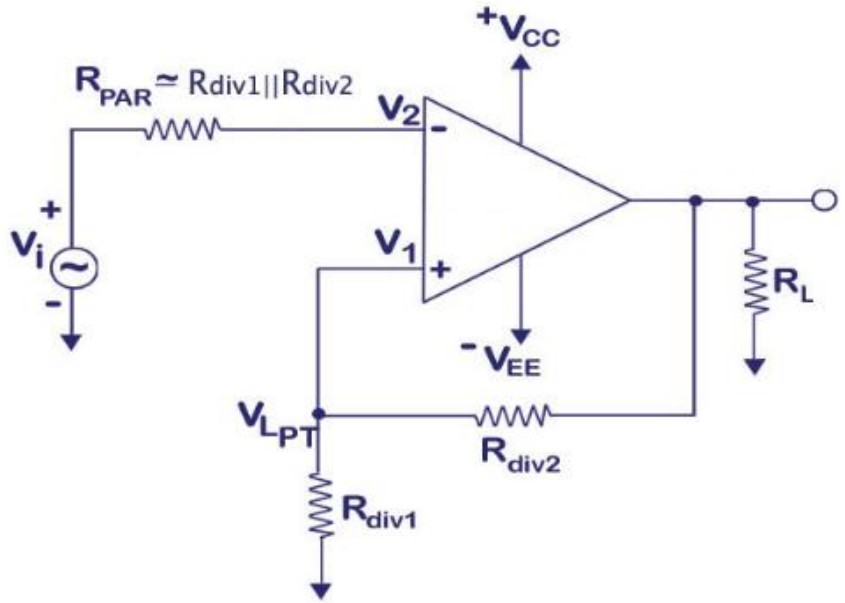
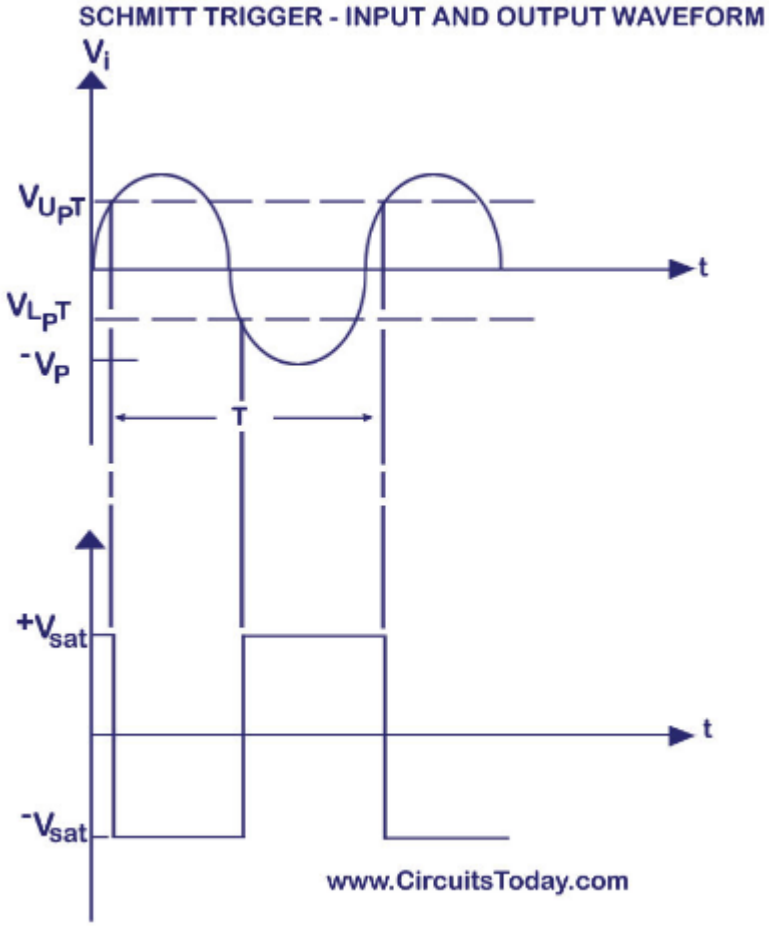
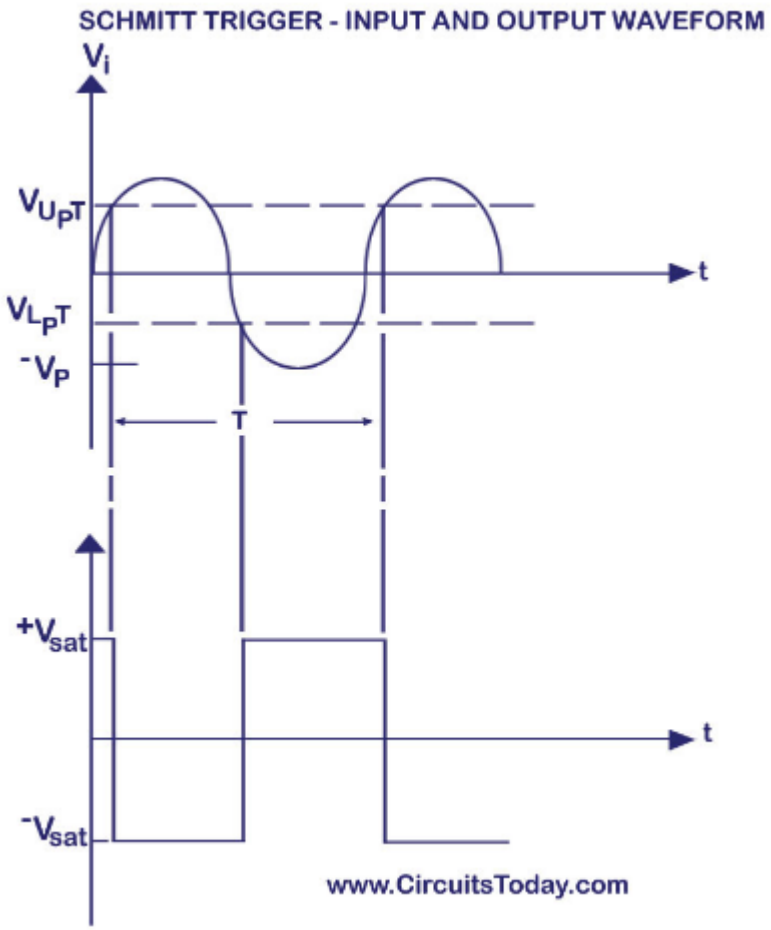


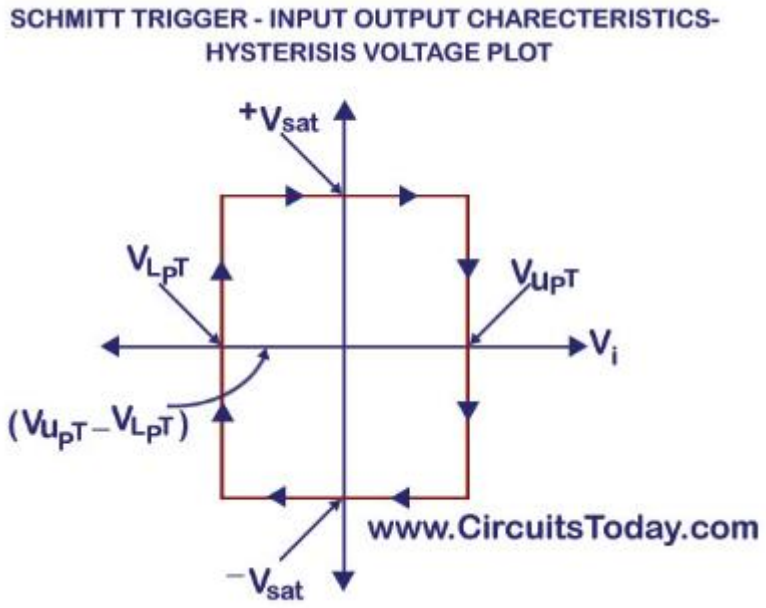


- If inverting input voltage has a slight positive value, a negative value wil apear at the output
- Which is fedback to the non-inverting terminal (+) of the op-amp
- Thus, value of the negative voltage becomes again higher until the circuit is driven into negative saturation (-Vsat)

- If inverting input voltage has a slight negative value, a positive value wil appear at the output
- which is fedback to the non-inverting terminal (+) of the op-amp through the voltage divider
- Thus, the value of the positive voltage that is fedback to the positive terminal becomes higher
- The value of the positive voltage becomes again higher until the circuit is driven into positive saturation (+Vsat)

Voltage Controlled Oscillator





- When the input of the comparator has a value higher than Vupt, its output switches from +Vsat to -Vsat
- Reverts back to its original state, +Vsat, when the input value goes below Vlpt.
- The hysteresis voltage can be calculated as the difference between the upper and lower threshold voltages.

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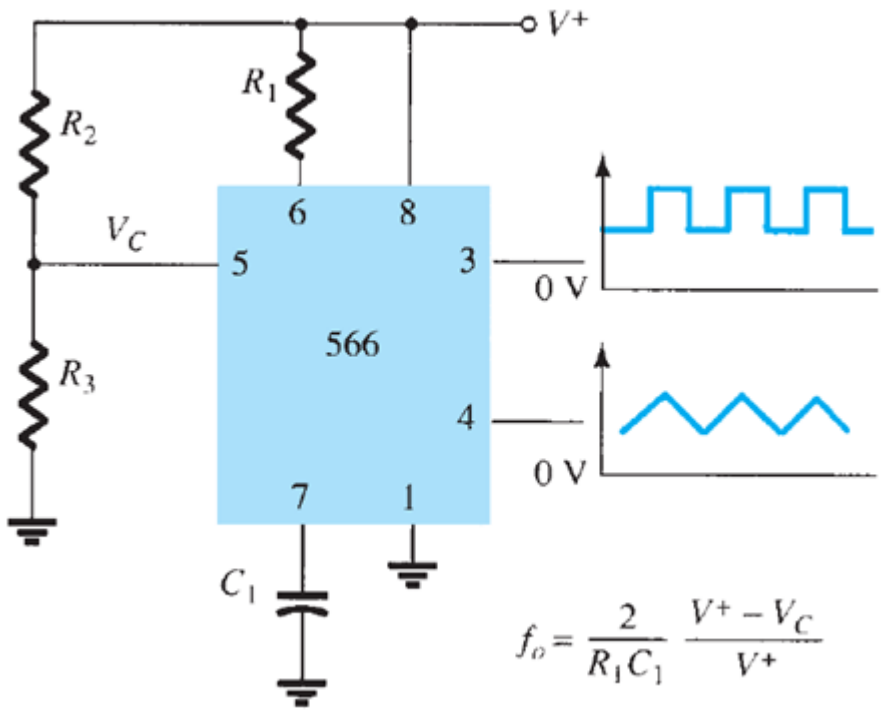
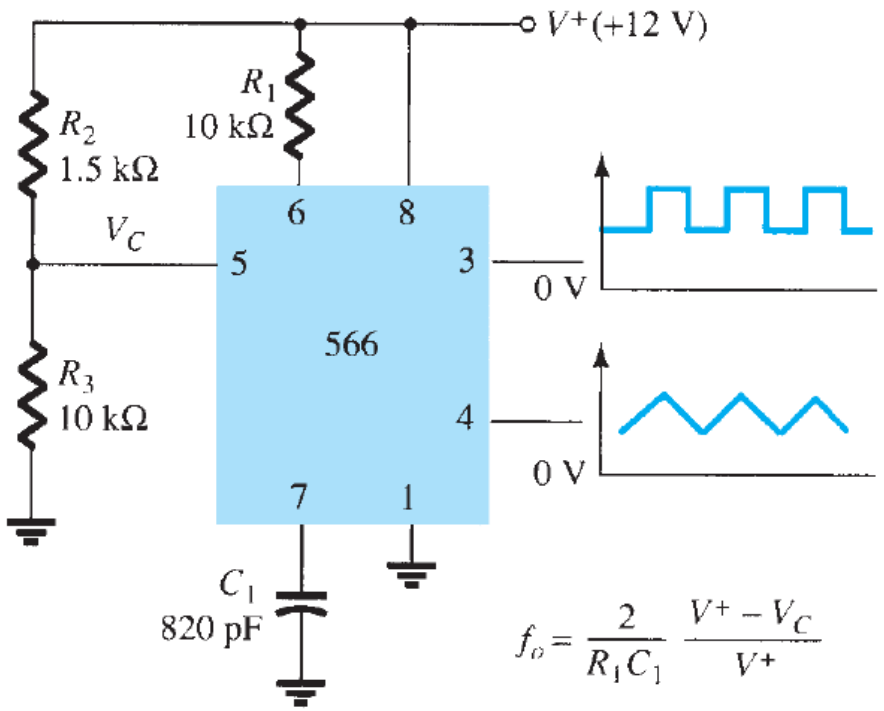


$$f_o = \frac{2}{R_1 C_1}\left(\frac{V^+ - V_C}{V^+}\right)$$

1. R_1 should be within the range $2\,\text{k}\Omega \leq R_1 \leq 20\,\text{k}\Omega$.
2. V_C should be within the range $\frac{3}{4}V^+ \leq V_C \leq V^+$.
3. f_o should be below 1 MHz.
4. V^+ should range between 10 V and 24 V.

Voltage Controlled Oscillator

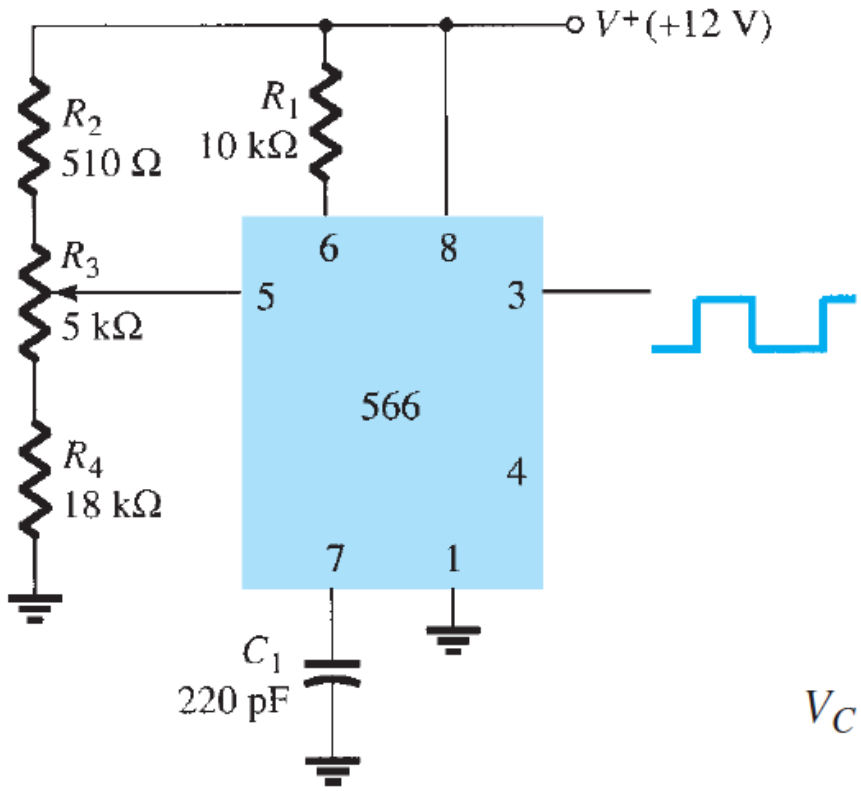


$$V_C = \frac{R_3}{R_2 + R_3} V^+ = \frac{10\,\text{k}\Omega}{1.5\,\text{k}\Omega + 10\,\text{k}\Omega}(12\,\text{V}) = 10.4\,\text{V}$$

which falls properly in the voltage range $0.75V^+ = 9\,\text{V}$ and $V^+ = 12\,\text{V}$

$$f_o = \frac{2}{(10 \times 10^3)(820 \times 10^{-12})}\left(\frac{12 - 10.4}{12}\right) \approx 32.5\,\text{kHz}$$

Voltage Controlled Oscillator



With the potentiometer wiper set at the top, the control voltage is

$$V_C = \frac{R_3 + R_4}{R_2 + R_3 + R_4}(V^+)$$

$$= \frac{5\,\text{k}\Omega + 18\,\text{k}\Omega}{510\,\Omega + 5\,\text{k}\Omega + 18\,\text{k}\Omega}(+12\,\text{V}) = 11.74\,\text{V}$$

$$f_o = \frac{2}{(10 \times 10^3)(220 \times 10^{-12})}\left(\frac{12 - 11.74}{12}\right) \approx 19.7\,\text{kHz}$$

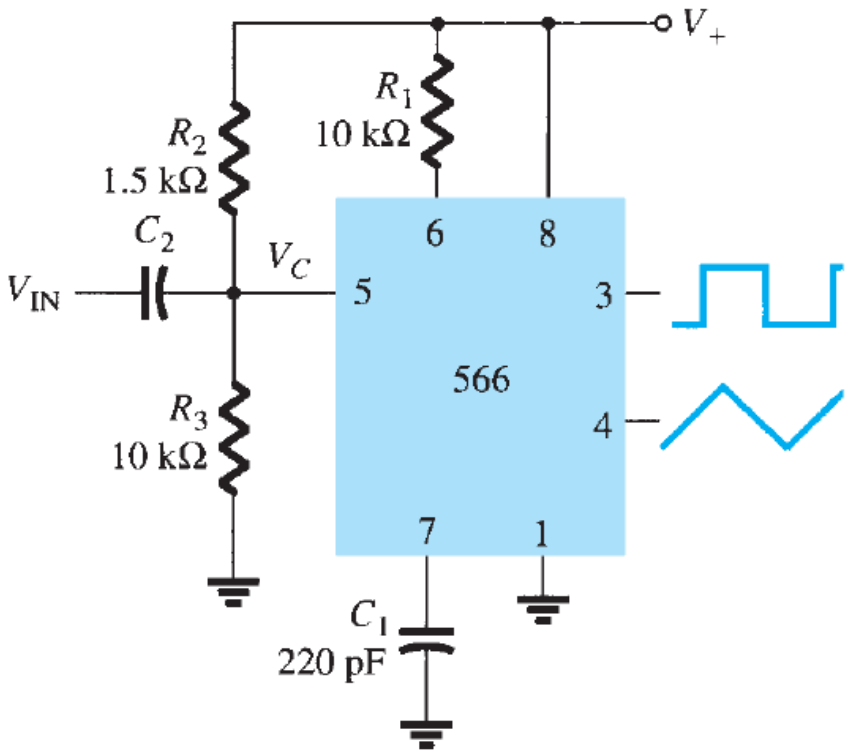
With the wiper arm of R_3 set at the bottom, the control voltage is

$$V_C = \frac{R_4}{R_2 + R_3 + R_4}(V^+) = \frac{18\,\text{k}\Omega}{510\,\Omega + 5\,\text{k}\Omega + 18\,\text{k}\Omega}(+12\,\text{V}) = 9.19\,\text{V}$$

$$f_o = \frac{2}{(10 \times 10^3)(220 \times 10^{-12})}\left(\frac{12 - 9.19}{12}\right) \approx 212.9\,\text{kHz}$$

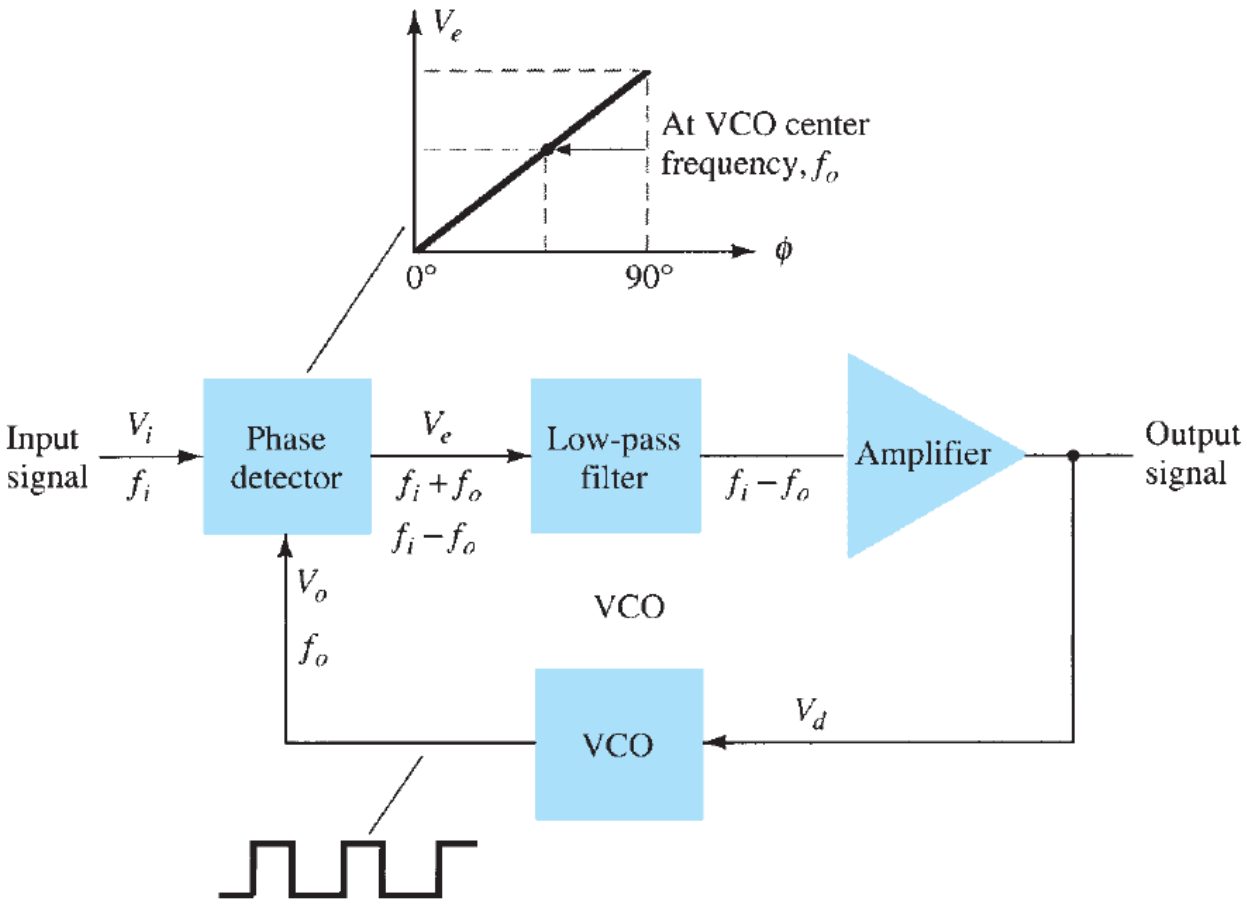
Voltage Controlled Oscillator

- Rather than varying a potentiometer setting to change the value of V_C , an input modulating voltage V_{in} can be applied as shown in the figure
- The voltage divider sets V_C at about 10.4 V
- An input ac voltage of about 1.4 V peak can drive V_C around the bias point between voltages of 9 V and 11.8 V, causing the output frequency to vary over about a 10-to-1 range
- The input signal *V in* thus frequency-modulates the output voltage around the center frequency set by the bias value of V_C = 10.4 V (f_o = 121.2 kHz)



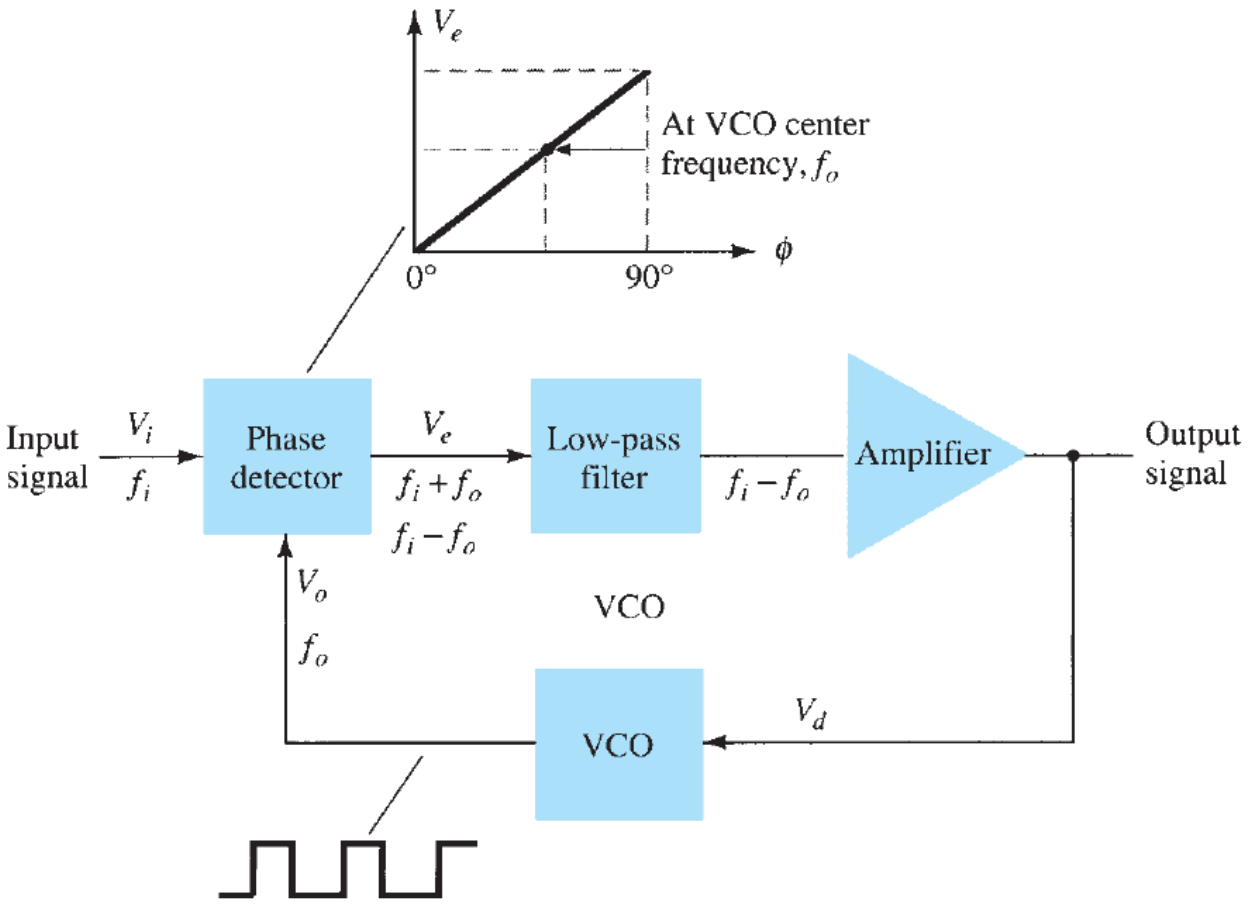
Phase-Locked Loop

- An input signal V_i and a signal from VCO, V_o, are compared by a phase comparator
- An output voltage V_e that represents the phase difference between the two signals is provided
- This voltage is then fed to a low-pass filter, which provides an output voltage (amplified if necessary) that can be taken as the output voltage from the PLL and is used internally as the voltage to modulate the VCO's frequency
- The closed-loop operation of the circuit is to maintain the VCO frequency locked to that of the input signal frequency.



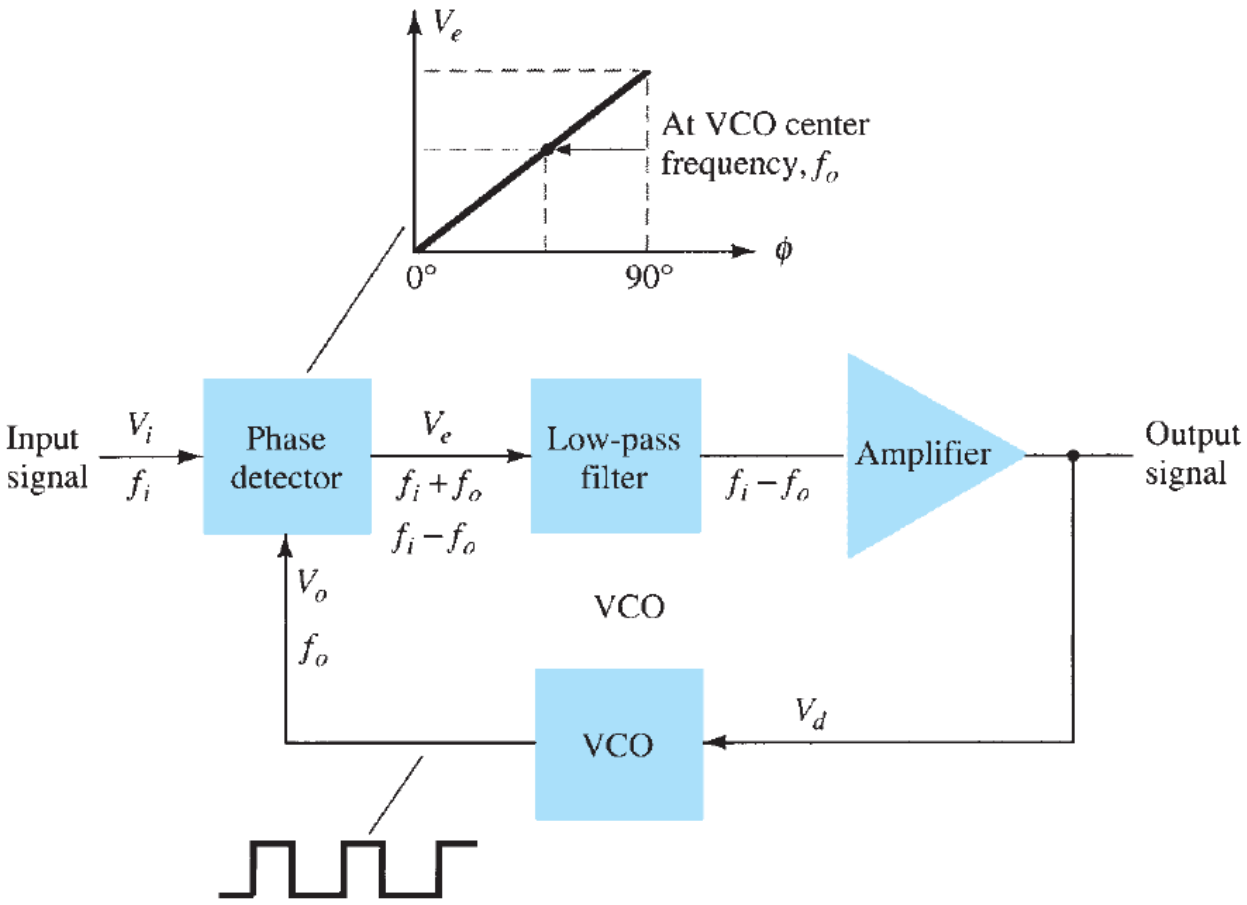
Phase-Locked Loop

- When the loop is in lock (input and VCO frequency are equal), V_d taken as output is the value needed to hold the VCO in lock
- VCO then provides a fixed-amplitude square-wave at the frequency of input
- When the loop is in lock, the two signals to the comparator are of the same frequency, although not necessarily in phase
- A fixed phase difference between the two signals to the comparator results in a fixed dc voltage to the VCO
- Changes in the input signal frequency then result in change in the dc voltage to the VCO
- Within a capture-and-lock frequency range, the dc voltage will drive the VCO frequency to match that of the input



Phase-Locked Loop

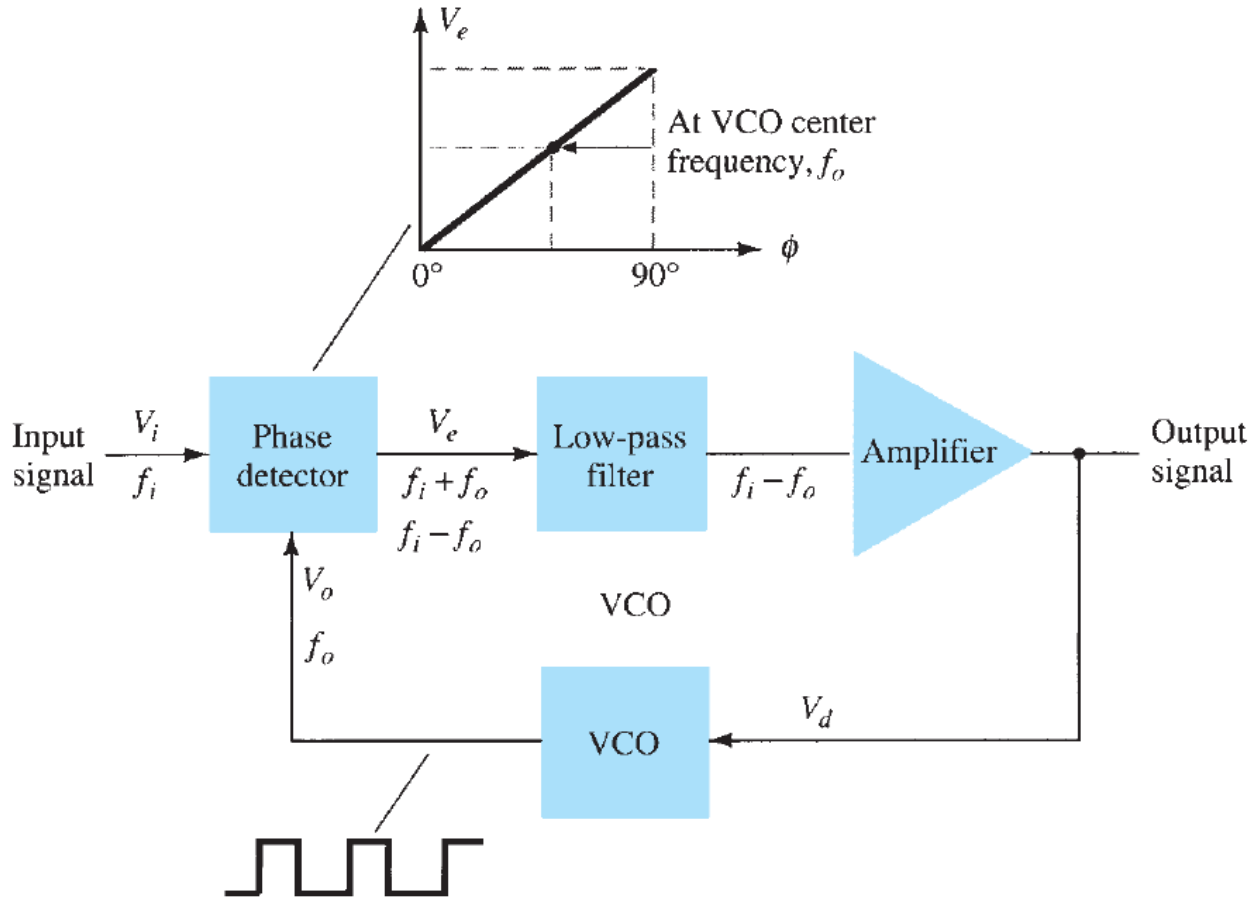
- While the loop is trying to achieve lock, the output of the phase comparator contains frequency components at the sum and difference of the signals compared
- A low-pass filter passes only the lower frequency component of the signal, so that the loop can obtain lock between input and VCO signals



Phase-Locked Loop - Applications

The PLL can be used in a wide variety of applications, including

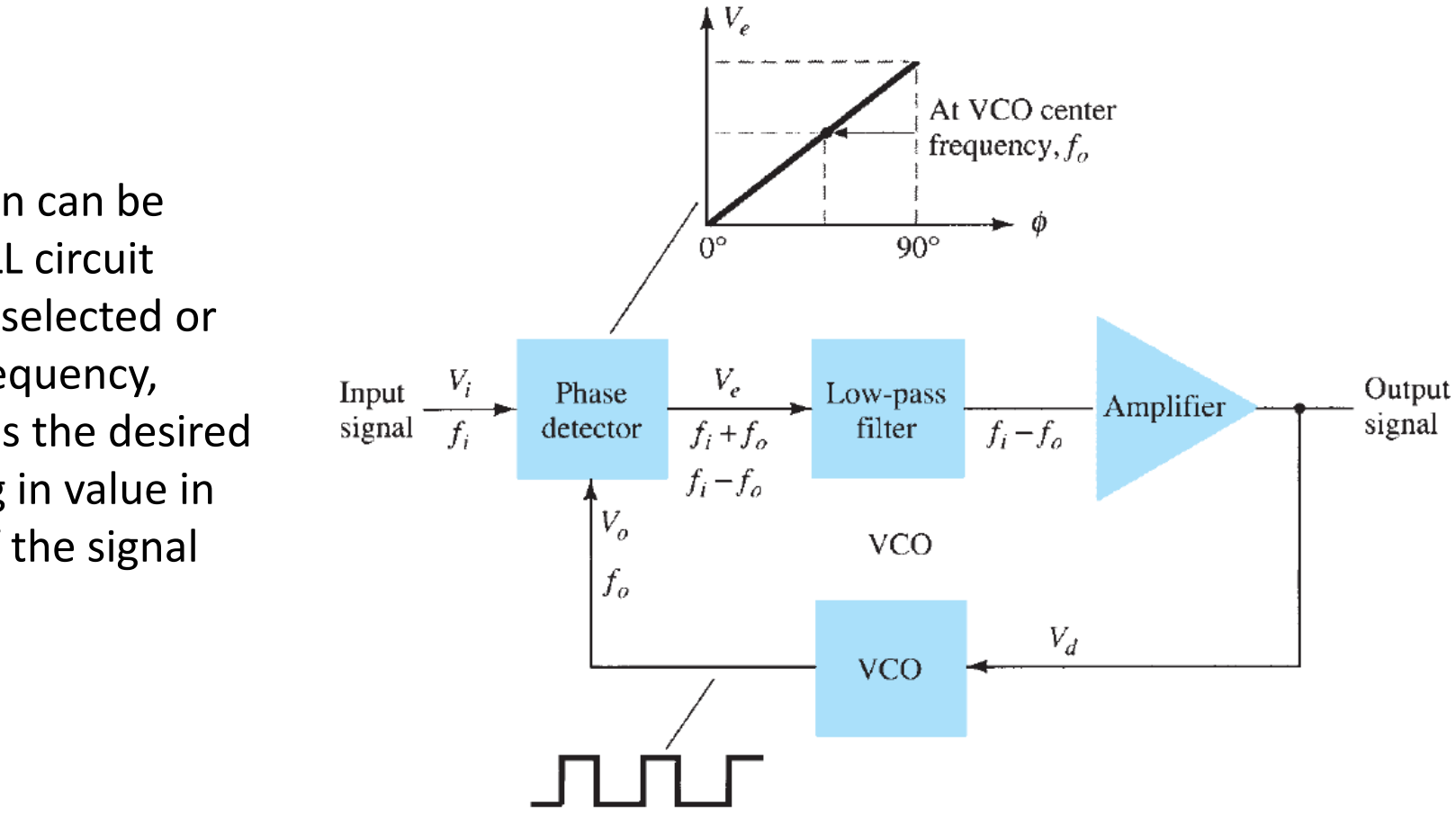
1. frequency demodulation,
2. frequency synthesis
3. FSK decoders.



Phase-Locked Loop - Applications

Frequency Demodulation

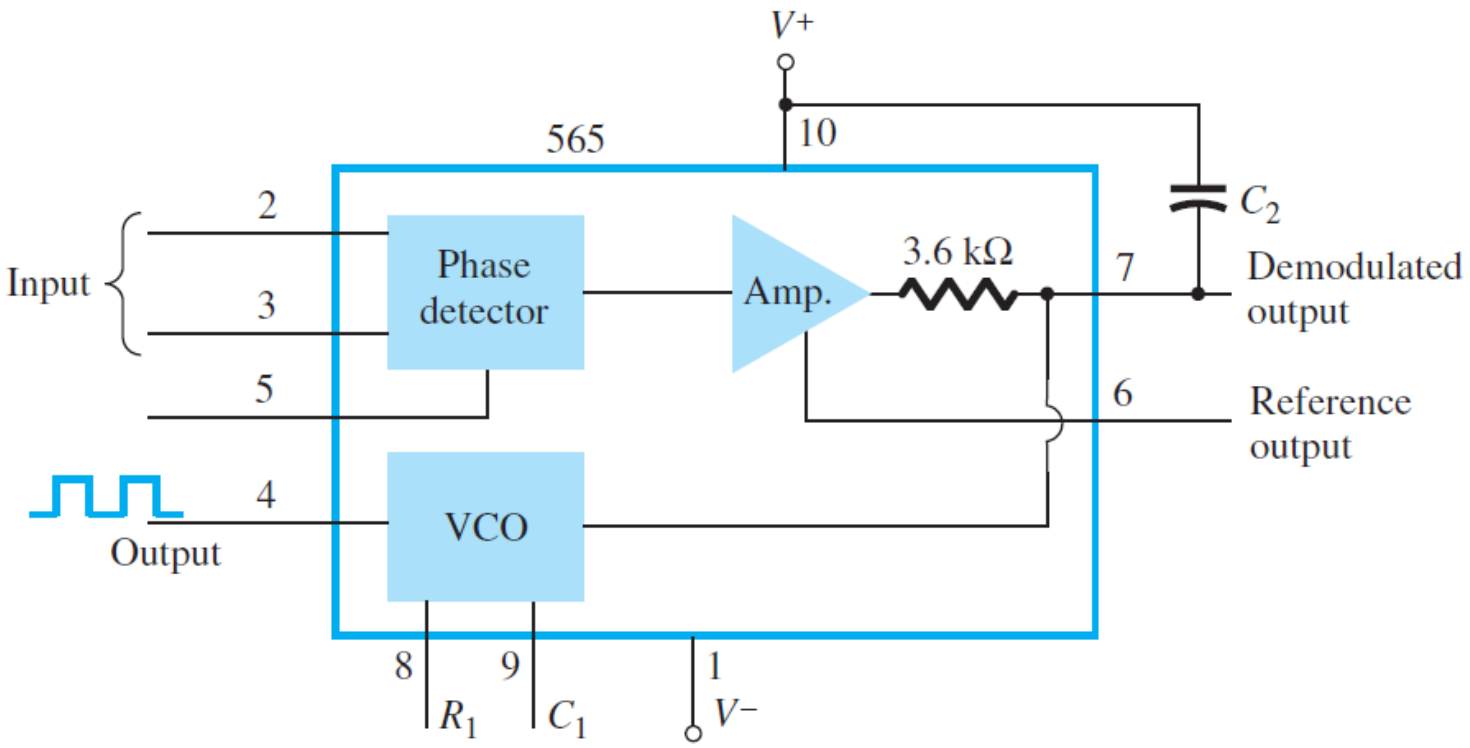
- FM demodulation or detection can be directly achieved using the PLL circuit
- If the PLL center frequency is selected or designed at the FM carrier frequency, filtered voltage of the circuit is the desired demodulated voltage, varying in value in proportion to the variation of the signal frequency



Phase-Locked Loop - Applications

Frequency Demodulation

- One popular PLL unit is the 565
- It contains a phase detector, an amplifier, and a voltage-controlled oscillator, which are only partially connected internally.
- An external resistor and capacitor R_1 and C_1 , respectively, are used to set the free-running or center frequency of the VCO.
- C_2 sets the low-pass filter passband
- VCO output must be connected back as input to the phase detector to close the PLL loop.
- The 565 typically uses two power supplies, V^+ and V^-



Phase-Locked Loop - Applications

Frequency Demodulation

- Figure shows PLL connected as an FM demodulator
- R_1 and C_1 set the free-running frequency f_o as follows:

$$\boxed{f_o = \frac{0.3}{R_1 C_1}}$$

$$= \frac{0.3}{(10 \times 10^3)(220 \times 10^{-12})}$$

$$= 136.36 \text{ kHz}$$

The lock range is

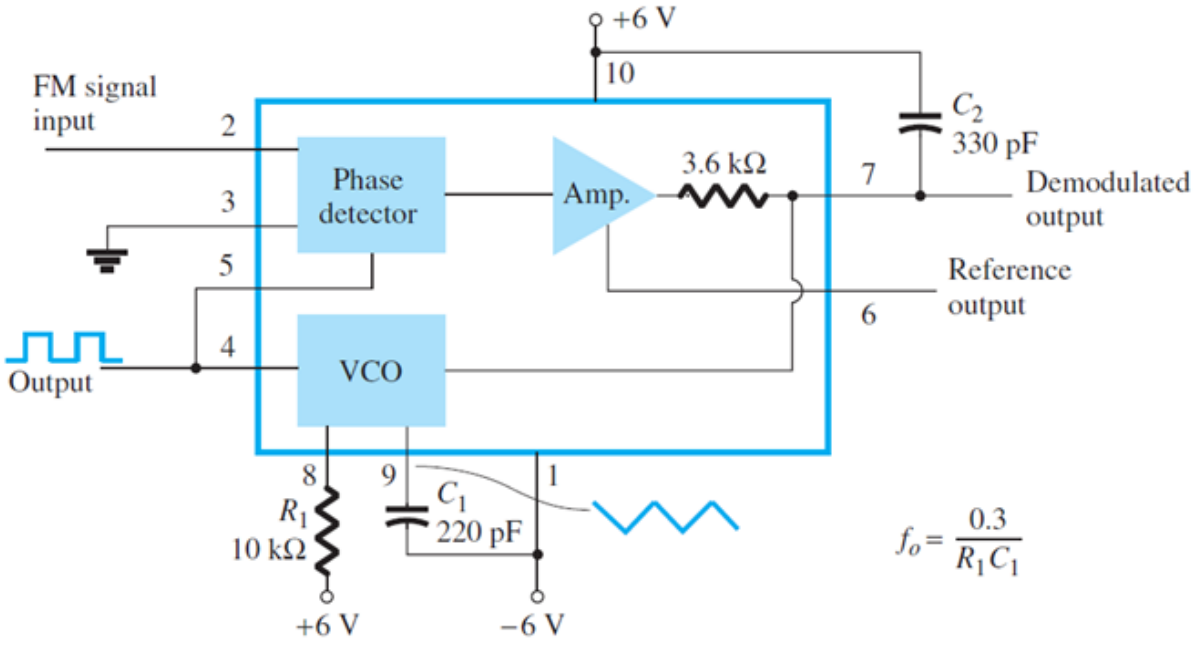
$$f_L = \pm \frac{8 f_o}{V}$$

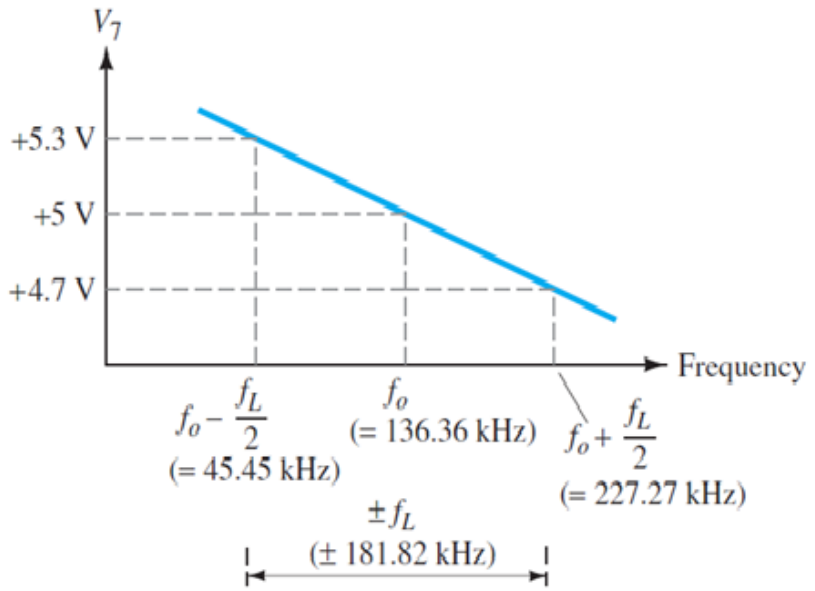
$$= \pm \frac{8(136.36 \times 10^3)}{6} = \pm 181.8 \text{ kHz}$$

The capture range is

$$f_C = \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{R_2 C_2}}$$

$$= \pm \frac{1}{2\pi} \sqrt{\frac{2\pi(181.8 \times 10^3)}{(3.6 \times 10^3)(330 \times 10^{-12})}} = 156.1 \text{ kHz}$$

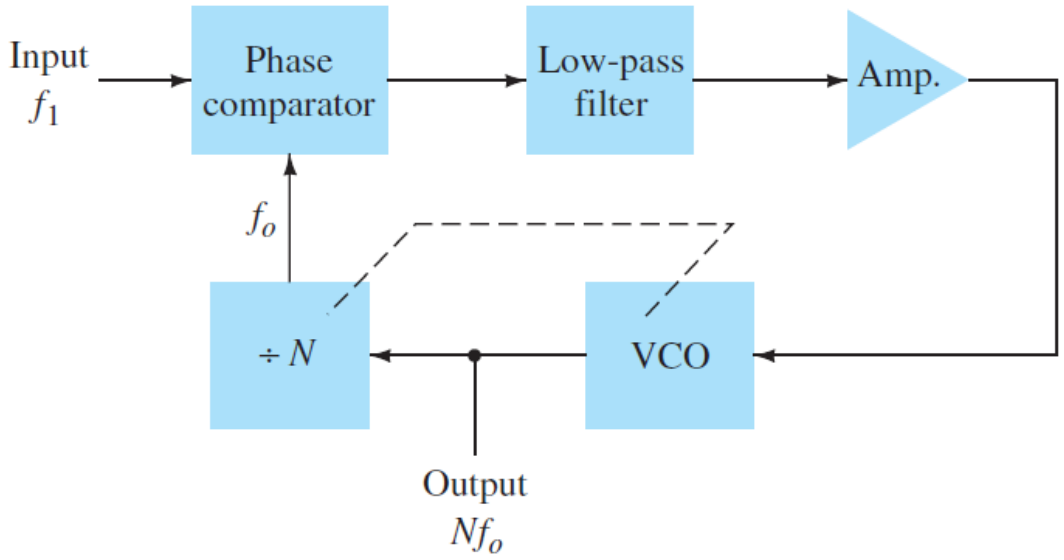




Phase-Locked Loop - Applications

Frequency Synthesis

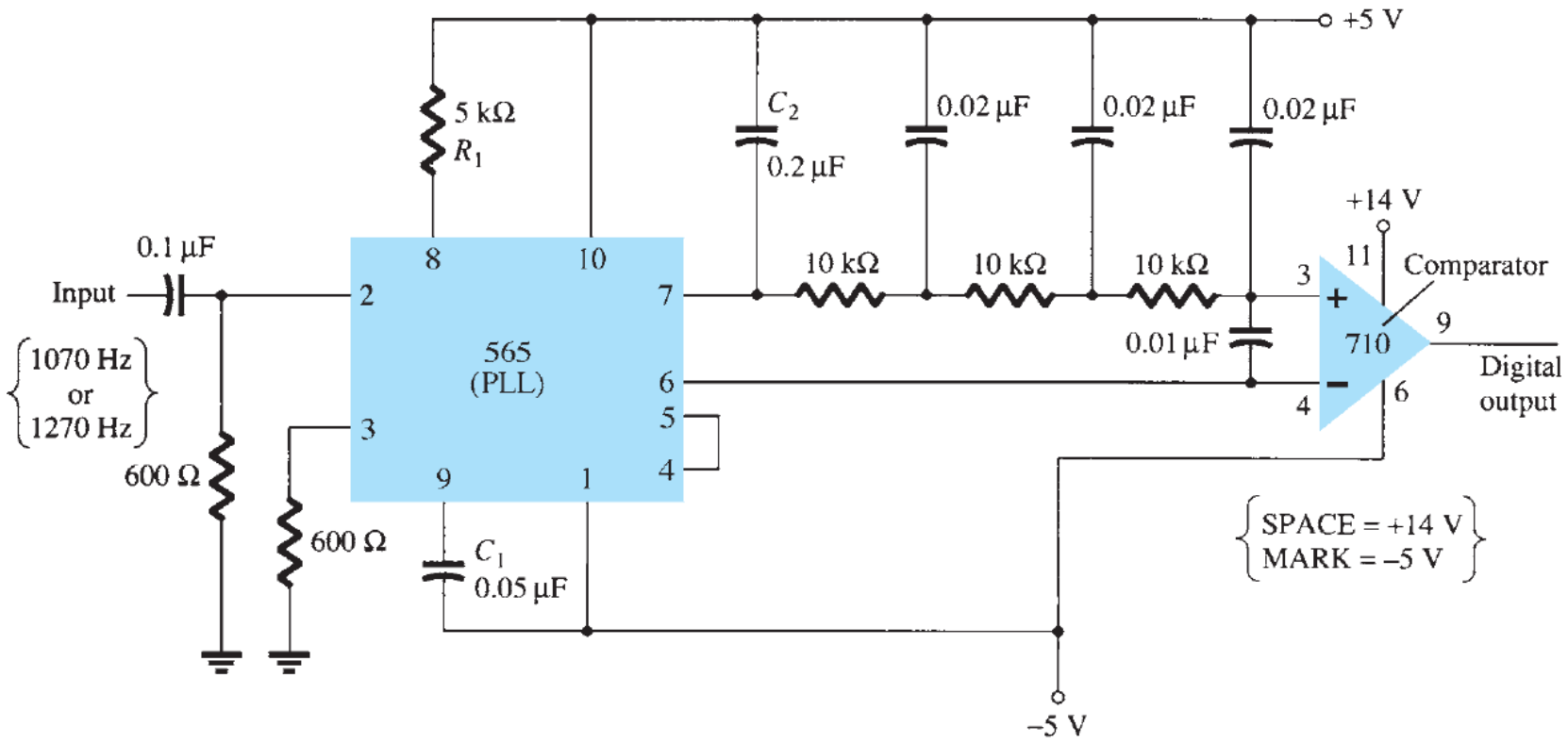
- A frequency divider is inserted between the VCO output and the phase comparator
- This causes loop signal to the comparator to be at f_o and the VCO output to be Nf_o
- This output is a multiple of the input frequency as long as the loop is in lock
- The input signal can be stabilized at f_1 with the resulting VCO output at Nf_1 if the loop is set up to lock at the fundamental frequency (when $f_o = f_1$)



Phase-Locked Loop - Applications

FSK Decoder

- Input carrier frequency is either 1270 or 1070 Hz
- Loop locks to the input frequency and tracks it between two possible frequencies with a corresponding dc shift at the output
- *RC* ladder filter (three sections of C = 0.02 mF and R = 10 k) removes the sum-frequency component



- Free-running frequency adjusted with R_1 so that the dc voltage level at pin 7 (output) is the same as that at pin 6
- Then an input at frequency 1070 Hz will drive the decoder output voltage to a more positive voltage level, driving the digital output to the high level (space, or 14 V)
- An input at 1270 Hz will correspondingly drive the 565 dc output less positive with the digital output, which then drops to the low level (5 V).