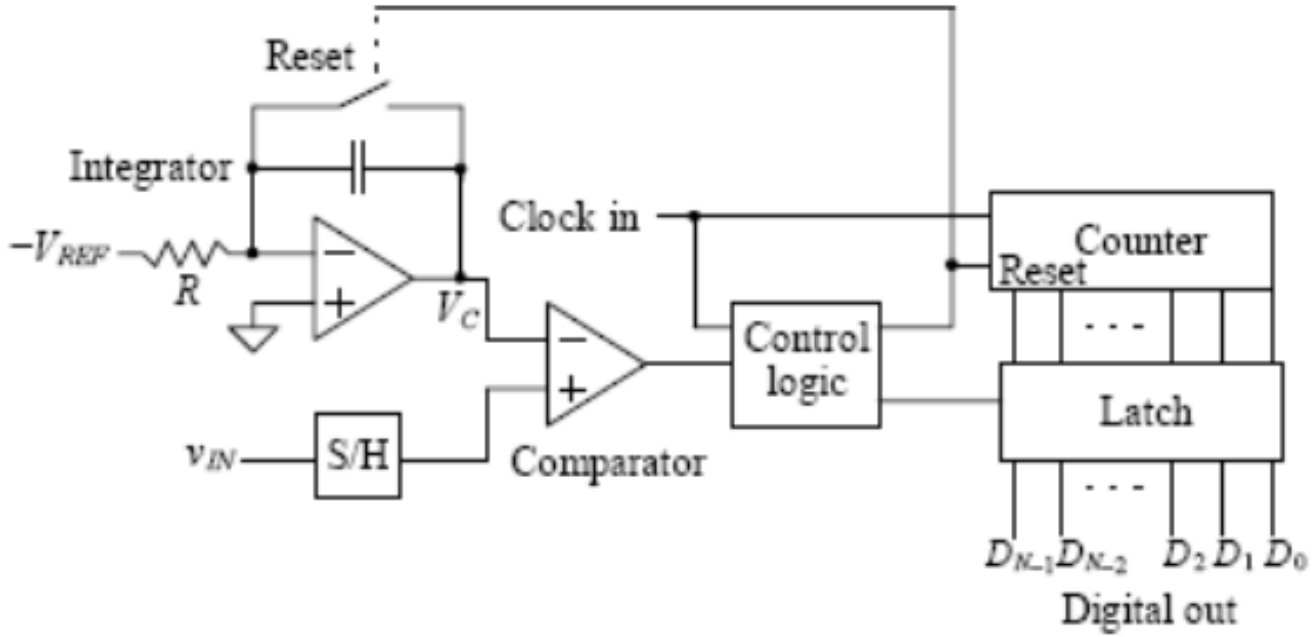
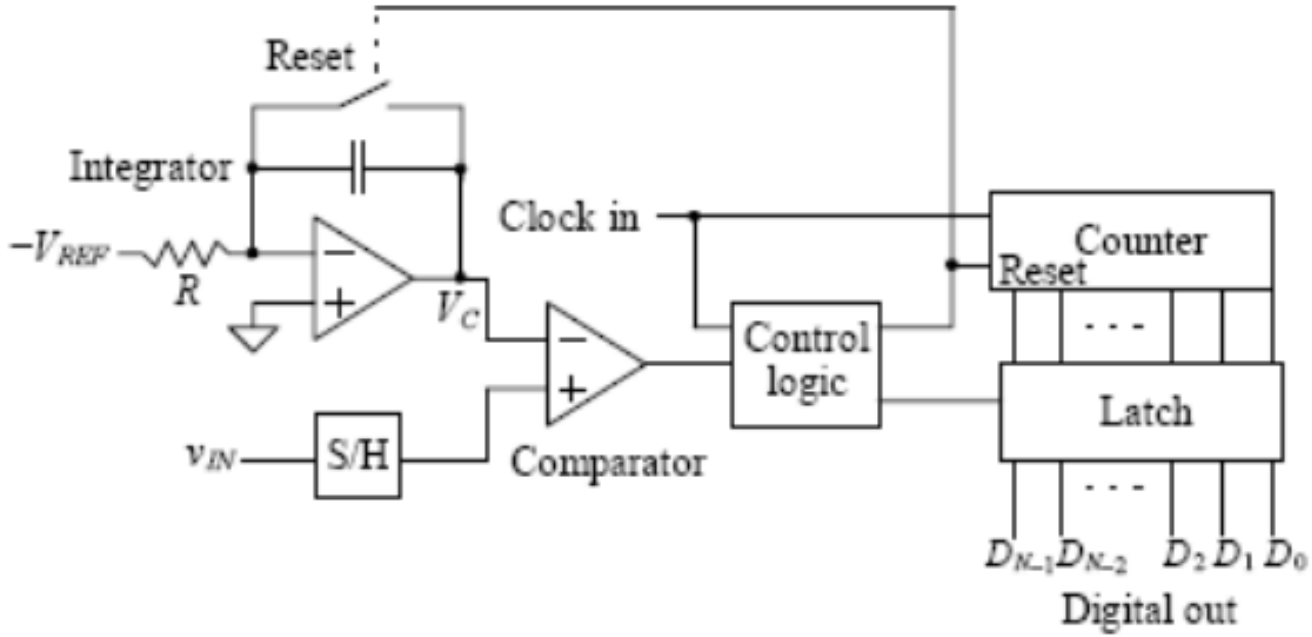
Linear Integrated Circuits

Single Slope ADC



- Comparator checks input voltage with integrated reference voltage, V_{REF}
- At the same time the number of clock cycles is being counted.
- When the integrator output equals V_{IN}, the comparator outputs a logic ‘0’, triggering the counter and integrator to reset and the latch to hold the digital output.

Single Slope ADC



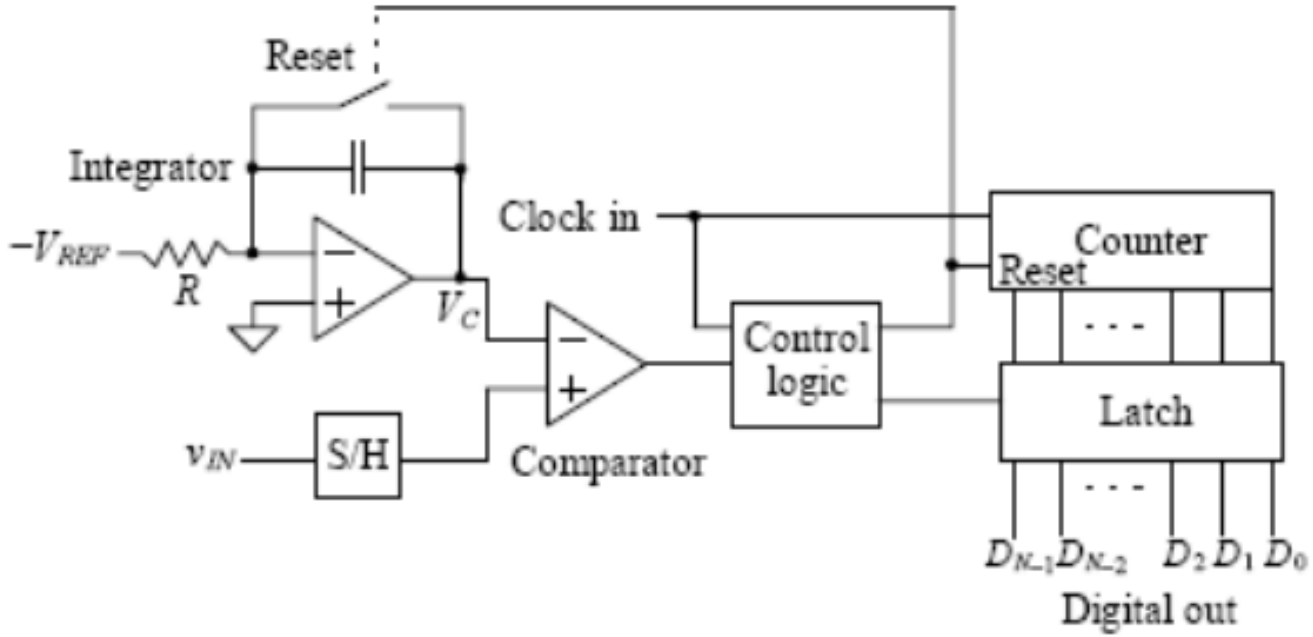
$$t_c = \frac{v_{in}}{\Delta V} T_{CLK}$$

$$= \frac{v_{in}}{V_{REF}} 2^N T_{CLK}$$

- ΔV the smallest change in analog signal that will result in a change in the digital output, also called «Resolution»

$$\Delta V = \frac{V_{\mathrm{REF}}}{2^N - 1} \approx \frac{V_{\mathrm{REF}}}{2^N} \quad \text{for large N}$$

Single Slope ADC

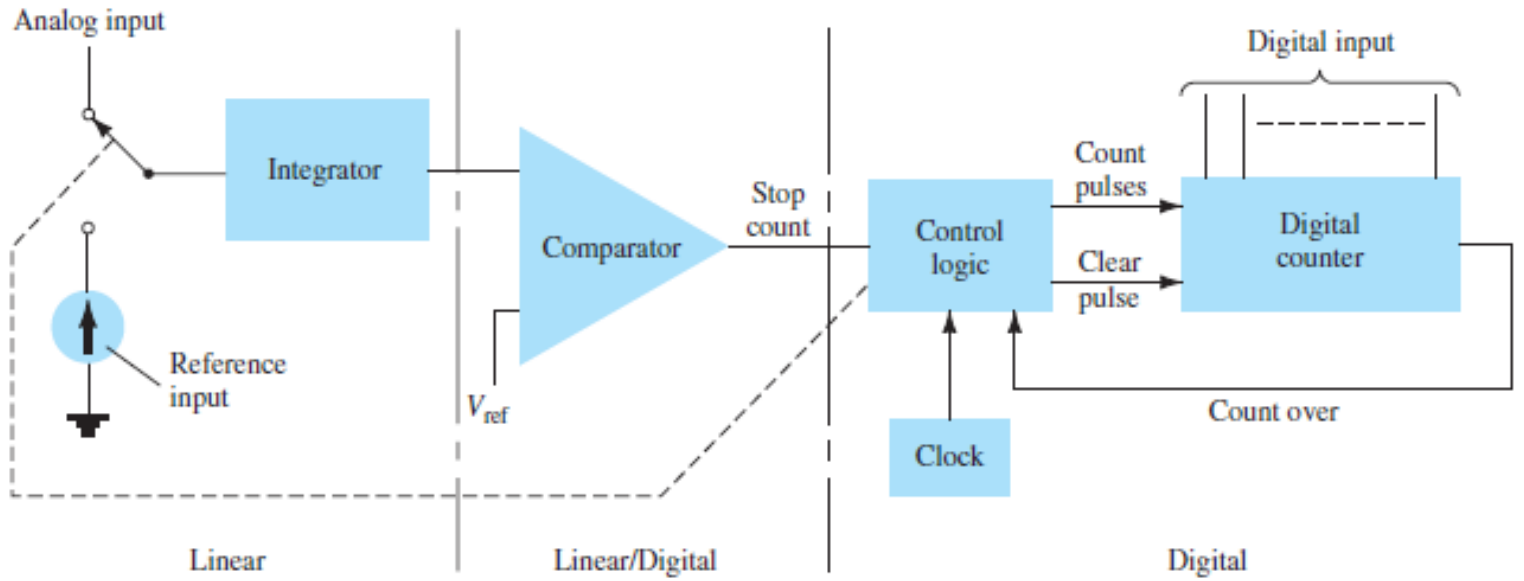


$$t_c = \frac{v_{in}}{\Delta V} T_{CLK}$$

$$= \frac{v_{in}}{V_{REF}} 2^N T_{CLK}$$

- Accuracy depends on tolerance of R and C.
- It would be better to develop an ADC whose accuracy does NOT depend on circuit element tolerances

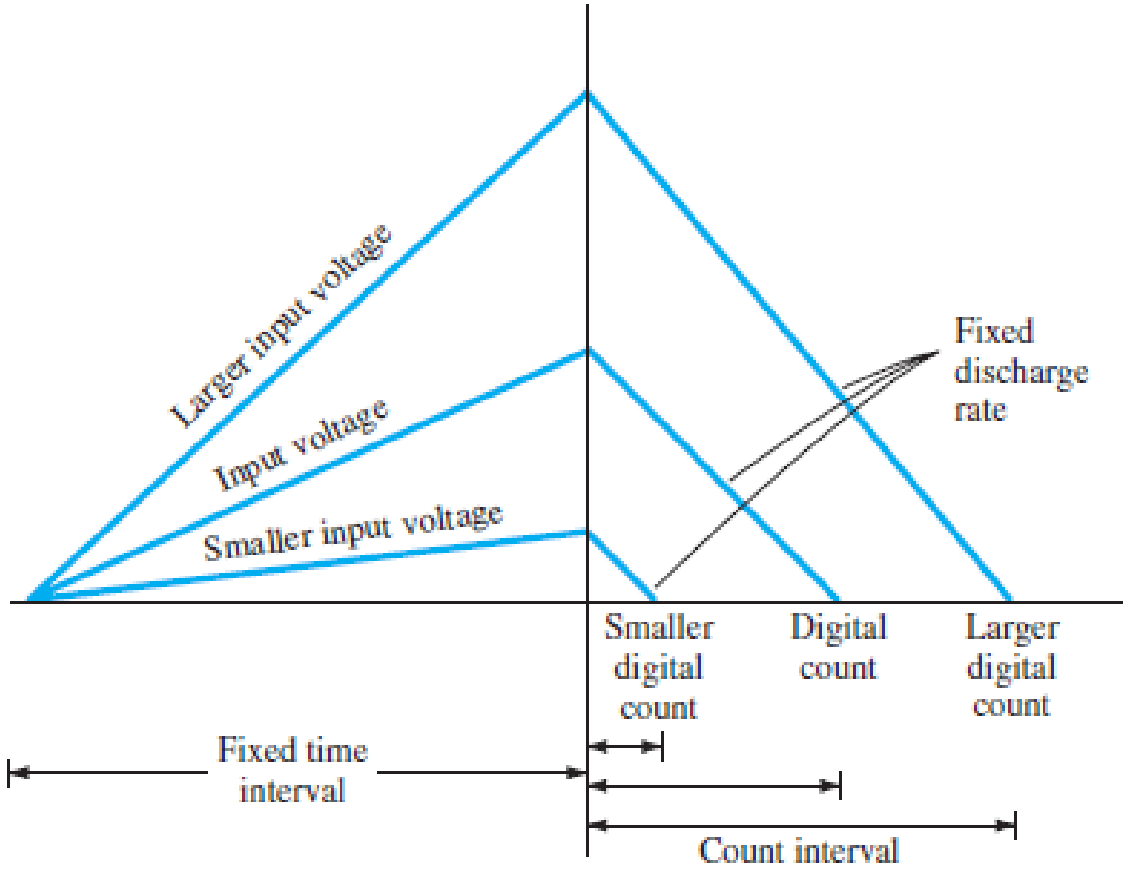
Dual Slope ADC



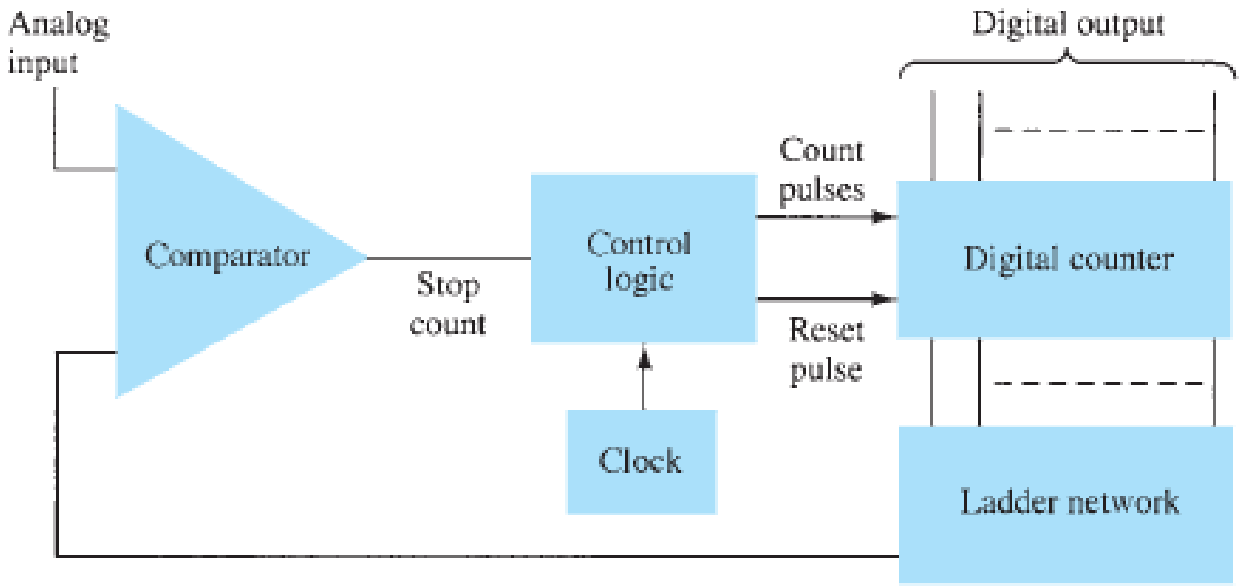
- For a **fixed time interval**, analog voltage connected to the integrator raises the voltage at the comparator input to some positive level
- At the end of this interval, count is set to zero and the electronic switch connects the integrator to a reference or fixed input voltage
- Then, counter advances whereas the integrator's output decreases at a **fixed rate** until it drops below the comparator reference voltage
- Then, control logic receives a signal (the comparator output) to stop the count
- Digital value stored in the counter is the digital output of the converter

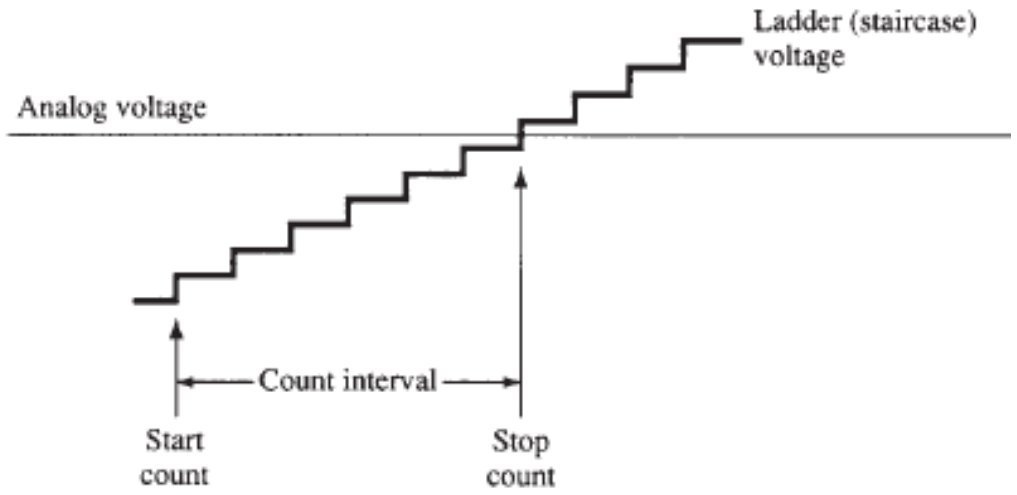
Dual Slope ADC

- For a **fixed time interval**, analog voltage connected to the integrator raises the voltage at the comparator input to some positive level
- At the end of this interval, the voltage from the integrator is greater for the larger input voltage
- Count is set to zero and the electronic switch connects the integrator to a reference or fixed input voltage
- Counter advances whereas the integrator's output decreases at a **fixed rate** until it drops below the comparator reference voltage



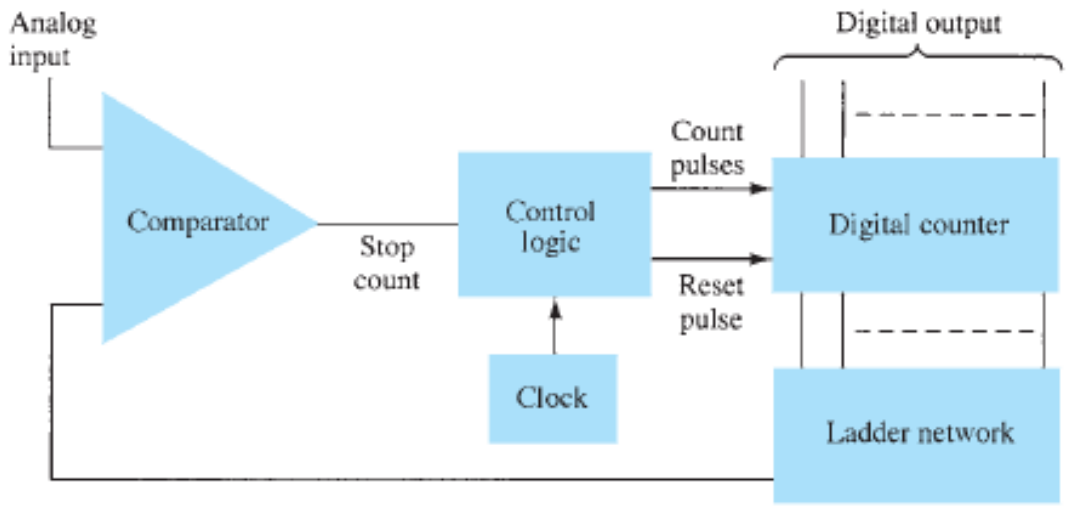
Ladder Network Conversion





- A digital counter advances from a zero count while a ladder network driven by the counter outputs a staircase voltage, as shown in right Fig., which increases one voltage increment for each count step
- A comparator circuit, receiving both staircase voltage and analog input voltage, provides a signal to stop the count when the staircase voltage rises above the input voltage
- The counter value at that time is the digital output

Ladder Network Conversion



- The amount of voltage change stepped by the staircase signal depends on the number of count bits used
- A 12-stage counter operating a 12-stage ladder network using a reference voltage of 10 V steps each count by a voltage of

$$\Delta V = \frac{V_{ref}}{2^{12} - 1} \approx \frac{10\ V}{4096} = 2.4\ mV$$

- The minimum number of conversions that could be carried out each second is then

$$\#conversions = \frac{1}{4.1} ms \approx 244\ conversions/second$$

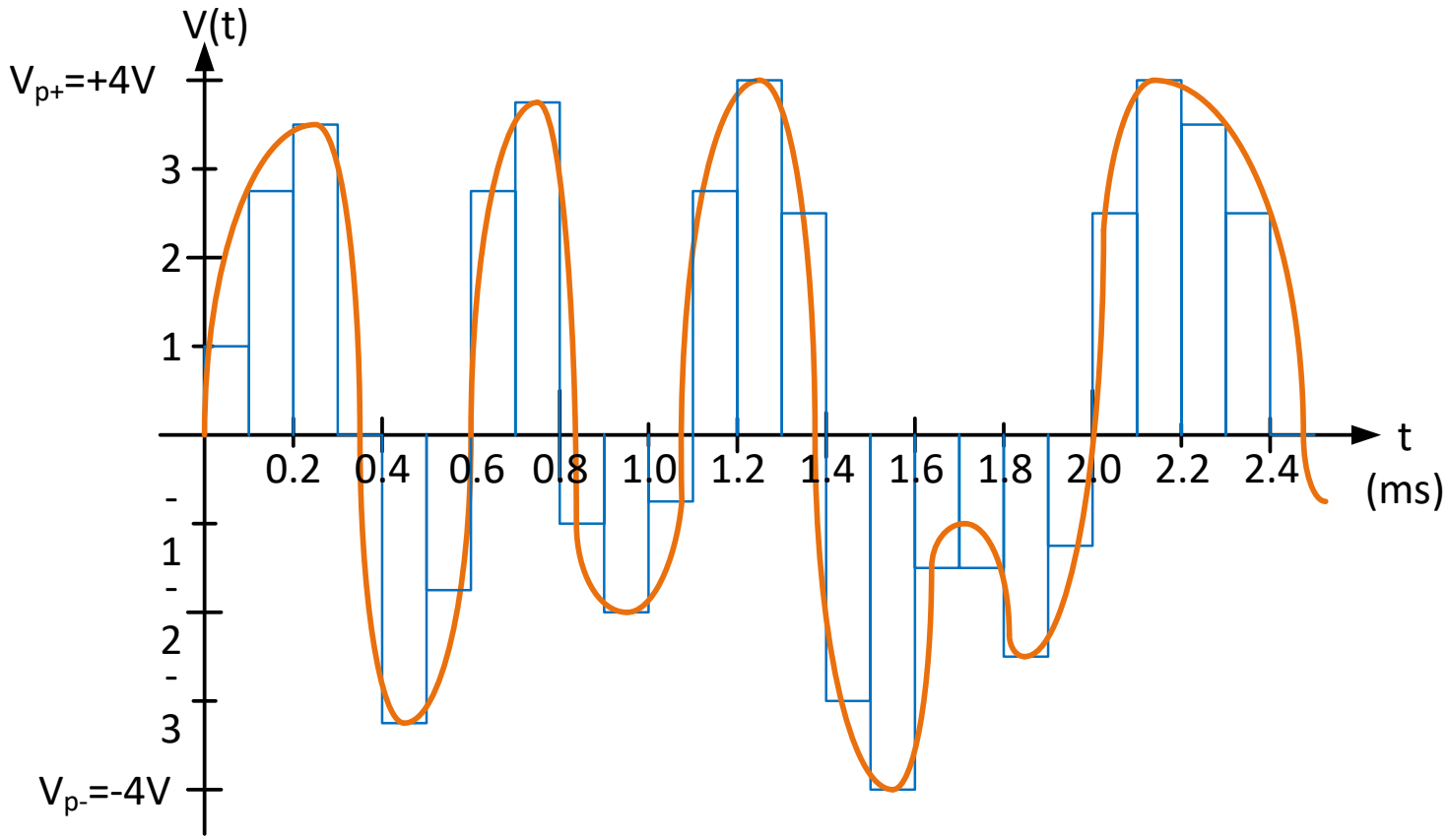
- Since a clock rate of 1 MHz operating a 12-stage counter needs a maximum conversion time of

$$4096 \times 1\mu s = 4096\mu s \approx 4.1ms$$

- Since on the average, with some conversions requiring little count time and others near maximum count time, a conversion time of $\frac{4.1ms}{2} = 2.05\ ms$ is needed,
- And the average number of conversions is $2 \times 244 = 488$ conversions/second
- A slower clock rate would result in fewer conversions per second
- A converter using fewer count stages (and less conversion resolution) would carry out more conversions per sec.
- The conversion accuracy depends on the accuracy of the comparator

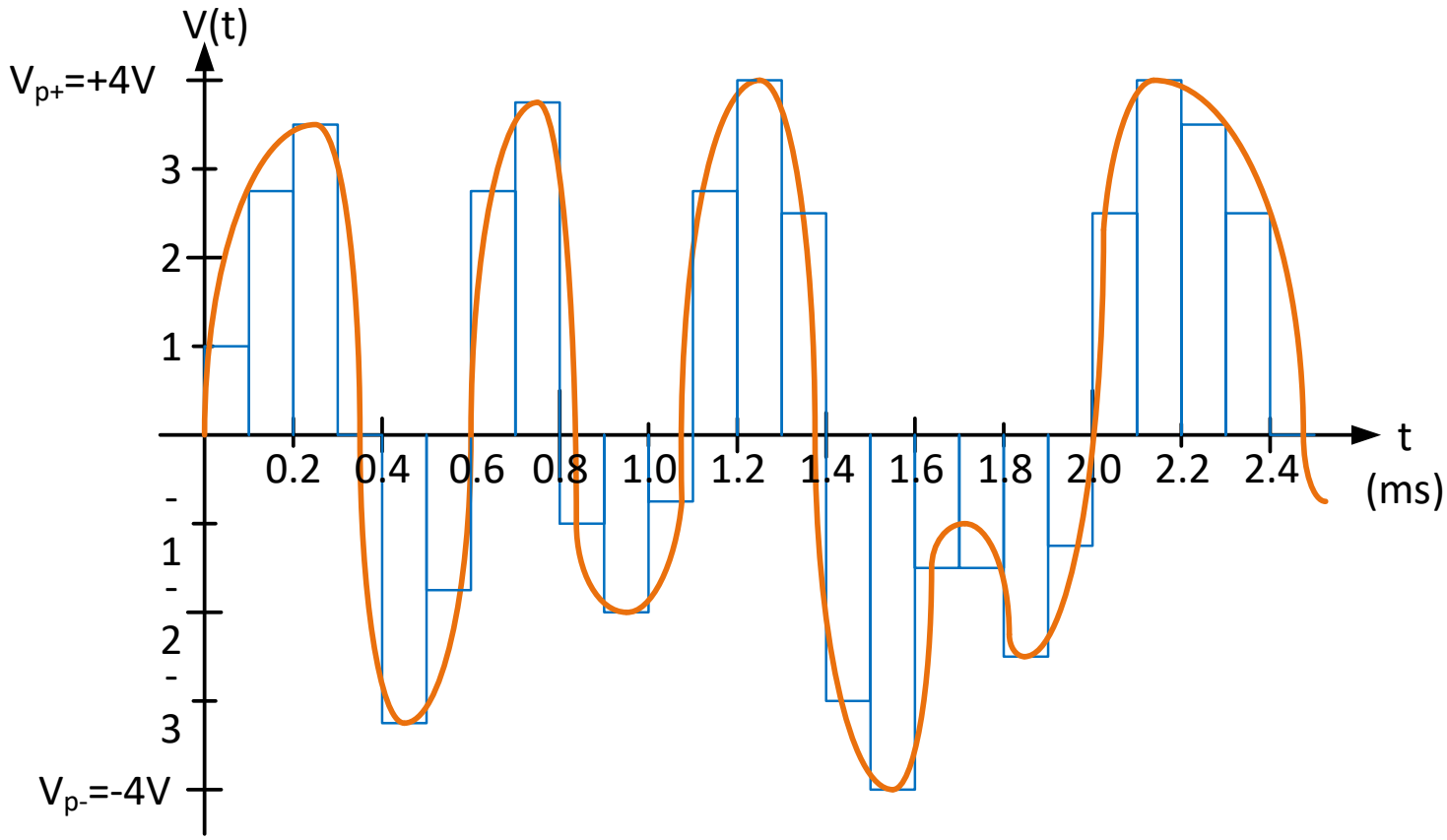
Analog to Digital Conversion Example

- A non-periodic analog signal
- Convert to a digital signal by using a 4-bit ADC
- What should be the sampling rate?
  - At least twice the highest frequency of the signal
  - But signal is NOT periodic
  - Cannot define a period or frequency of the signal
  - Instead we should take the bandwidth of the signal
  - Sampling rate at least twice the bandwidth
  - i.e. $f_S = \frac{1}{T_S} \geq 2\ BW$ (Nyquist criterion)



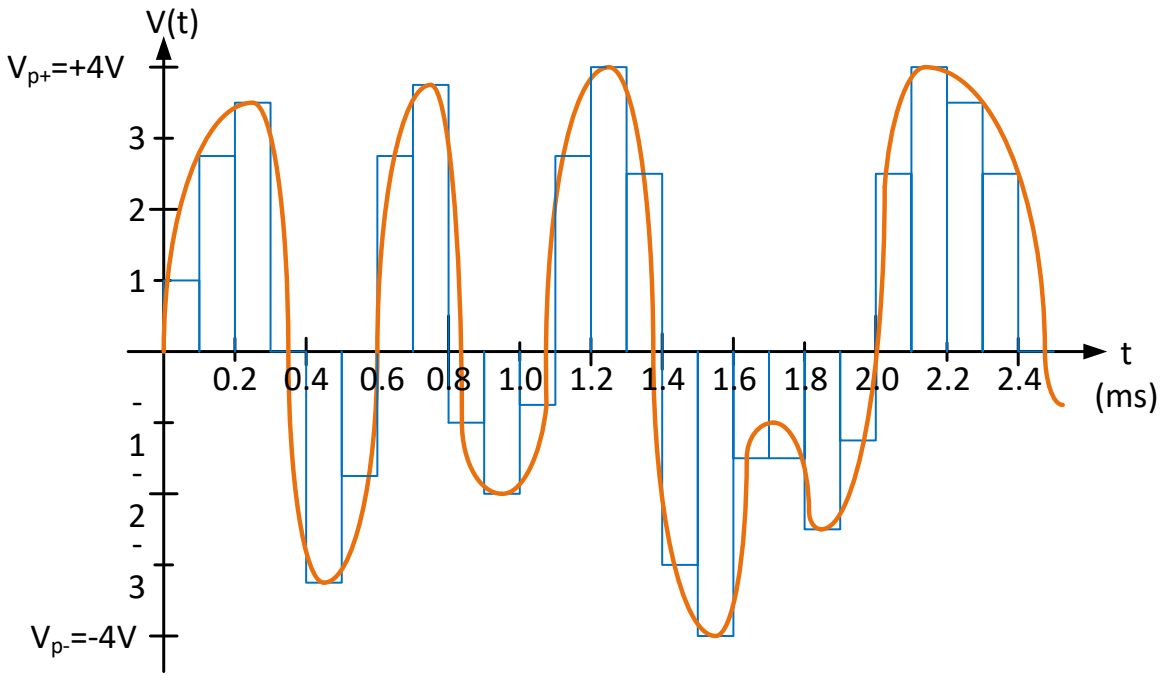
Analog to Digital Conversion Example

- Sampling
  - Let's take $T_s = 1\ ms$ (Assuming it satisfies Nyquist criterion $f_s = \frac{1}{T_s} \geq 2\ BW$)
  - We take samples at each T_s
- Quantization
  - The sampled value of the analog signal is kept constant via a sample and hold circuit.
  - These values will be represented by the combinations that can be obtained by using 4-bits (N=4)



Analog to Digital Conversion Example

- $\Delta V = \frac{V_{\max} - V_{\min}}{2^N - 1} = \frac{4-(-4)}{2^4-1} = \frac{8}{15} = 0.53\ V$



Analog Signal Level ***Digital Word***

$-3.99\ V \rightarrow 1111$
$+3.46\ V \rightarrow 1110$
$+2.92\ V \rightarrow 1101$
$+2.38\ V \rightarrow 1100$
$+1.85\ V \rightarrow 1011$
$+1.32\ V \rightarrow 1010$
$+0.79\ V \rightarrow 1001$
$+0.26\ V \rightarrow 1000$
$-0.28\ V \rightarrow 0111$
$-0.81\ V \rightarrow 0110$
$-1.34\ V \rightarrow 0101$
$-1.88\ V \rightarrow 0100$
$-2.41\ V \rightarrow 0011$
$-2.94\ V \rightarrow 0010$
$-3.47\ V \rightarrow 0001$
$-4.00\ V \rightarrow 0000$

Sample #	Signal value	Quant. value	Digital word
S1	+1 V	+0.79	1001
S2	+2.5 V	+2.38	1100
S3	+3 V	+2.92	1101
S4	0 V	-0.28	0111
S5	-3.2 V	-3.47	0001
S6	-1.98 V	-2.41	0011
S7	+2.6 V	+2.38	1100
S8	+3.8 V	+3.46	1110
…	…	…	…

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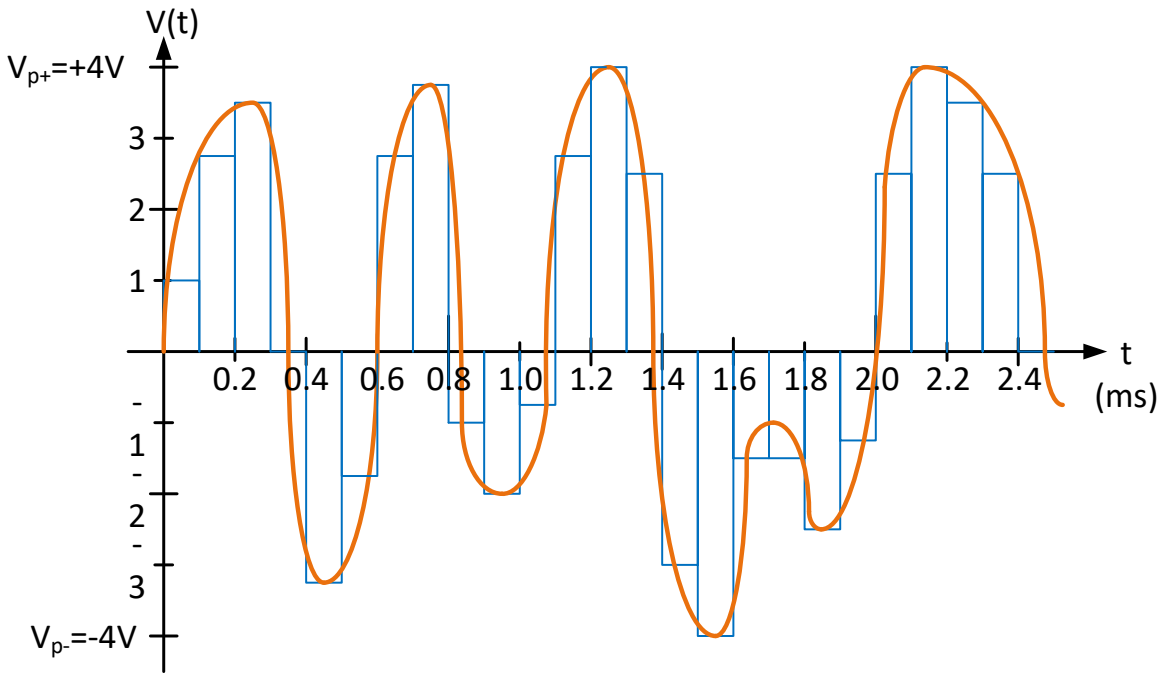

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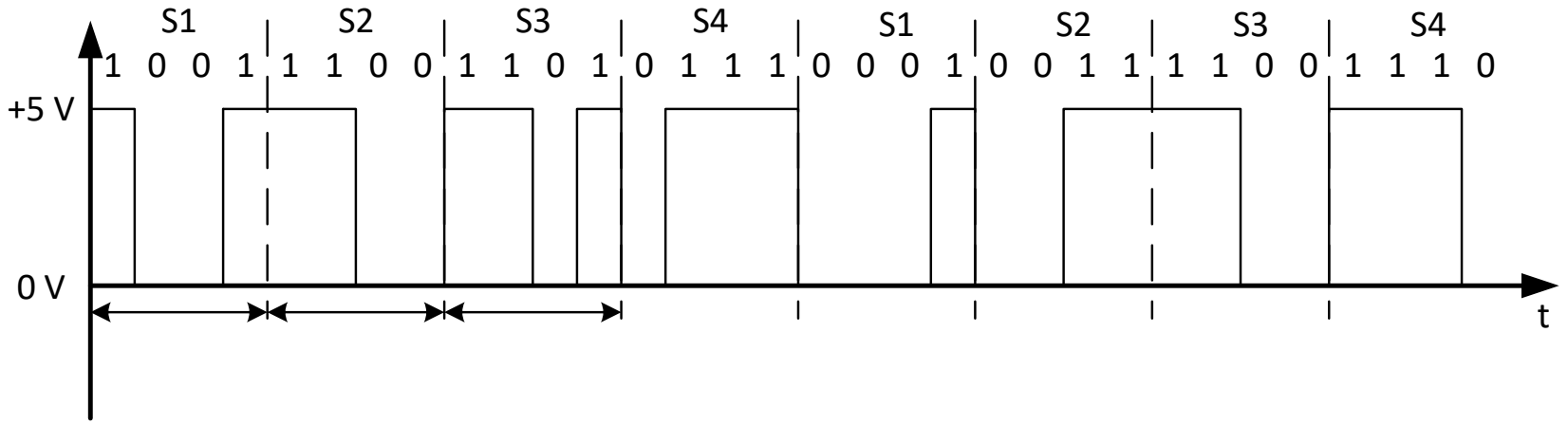
$-3.47\ V$	$\rightarrow 0001$
$-4.00\ V$	$\rightarrow 0000$

- S1 =1V does NOT exist among analog signal levels that can be represented by a 4-bit word.
- We have to choose among available values
- 1V is between two quantized values: +0.79 and +1.32
- We choose the lowest one as a rule here.

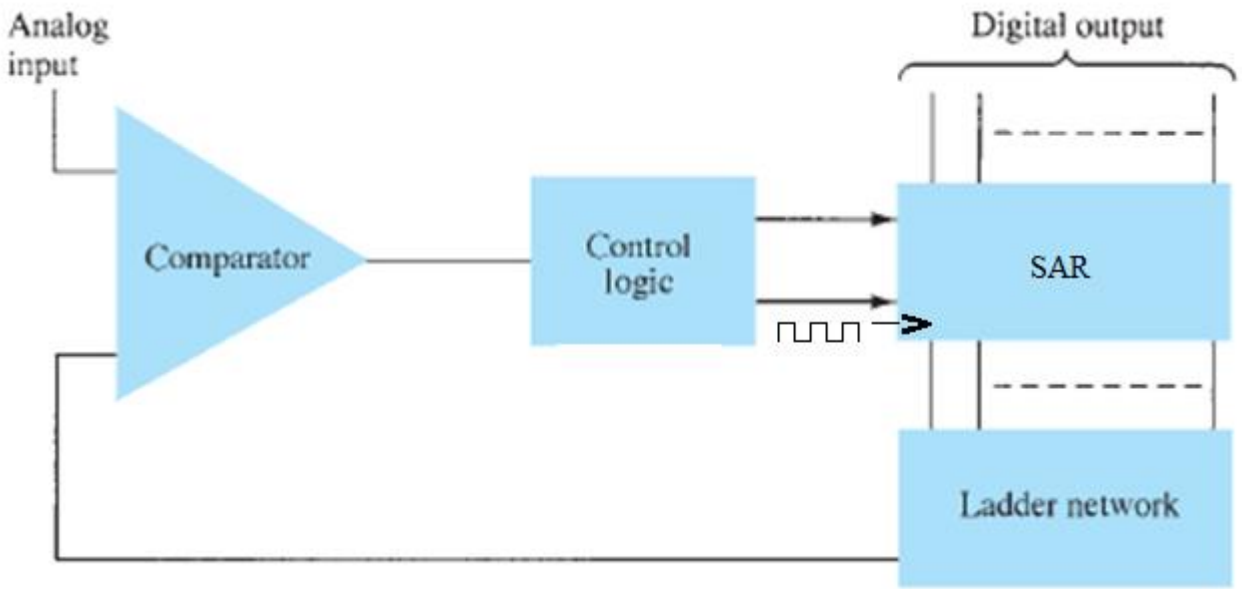
Analog to Digital Conversion Example



- If one bit is generated in 1 clock cycle of the ADC,
- To represent each signal sample, we need 4 clock cycles
- We can fasten conversion of each analog signal by increasing the clock frequency.

Successive Approximation ADC

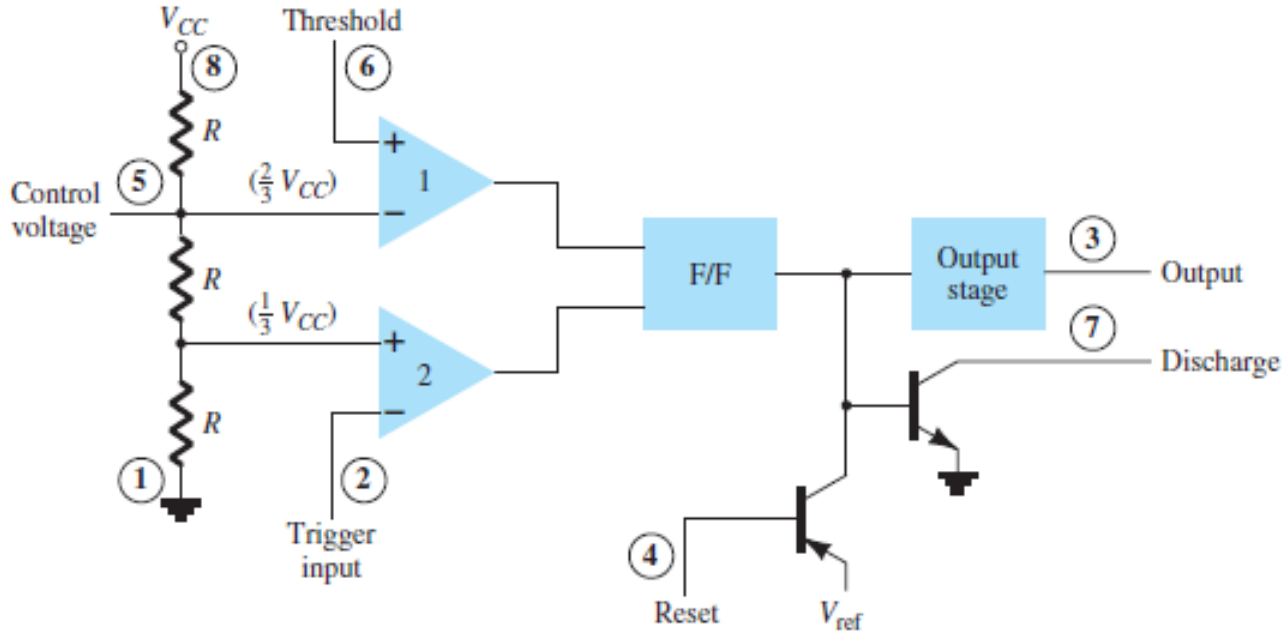
- Initially, the successive approximation register (SAR) is set to a value where only the most significant bit (MSB) is equal to 1, all other bits zero.
- This code is fed into the ladder network,
- The ladder network provides the analog equivalent of this digital code (Vref/2)



- Comparator checks it with the sampled input voltage level
- If this analog voltage exceeds V_{in}, the comparator causes the SAR to reset this bit
- Otherwise, the bit is left as 1 and next bit is set to 1 and the same test is done
- This goes on until every bit in the SAR has been tested
- The resulting code is the digital approximation of the sampled input

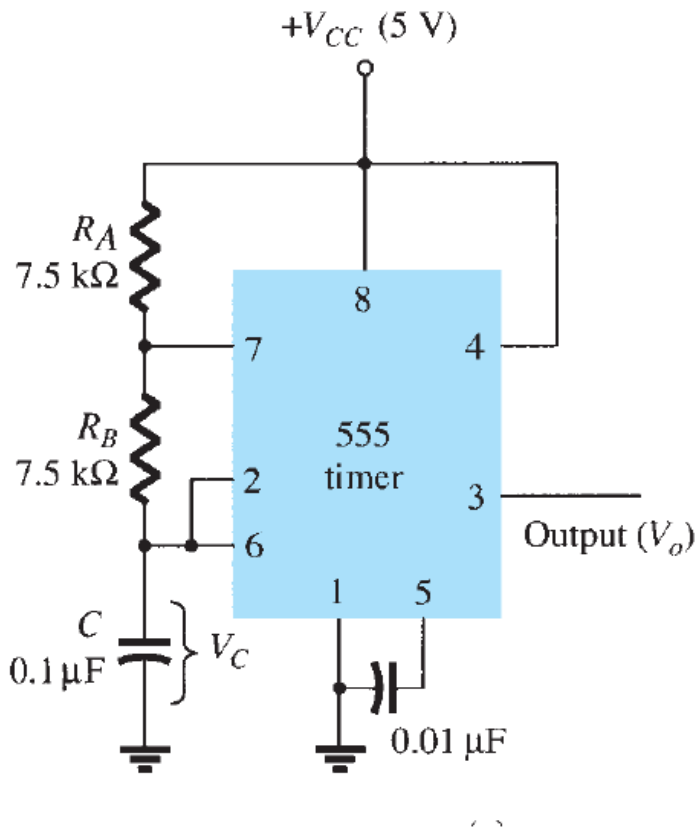
Timer IC Unit Operation

- Capacitor C charges toward V_{CC} through external resistors R_A and R_B
- Capacitor voltage rises until it goes above $2V_{CC}/3$
- This is the threshold voltage at pin 6, which drives comparator 1 to trigger the flip-flop so that the output at pin 3 goes low
- In addition, the discharge transistor is driven on, causing the output at pin 7 to discharge the capacitor through resistor R_B



- The capacitor voltage then decreases until it drops below the trigger level ($V_{CC}/3$)
- The flip-flop is triggered so that the output goes back high and the discharge transistor is turned off, so that the capacitor can again charge through resistors R_A and R_B toward V_{CC} .

Timer IC Unit Operation

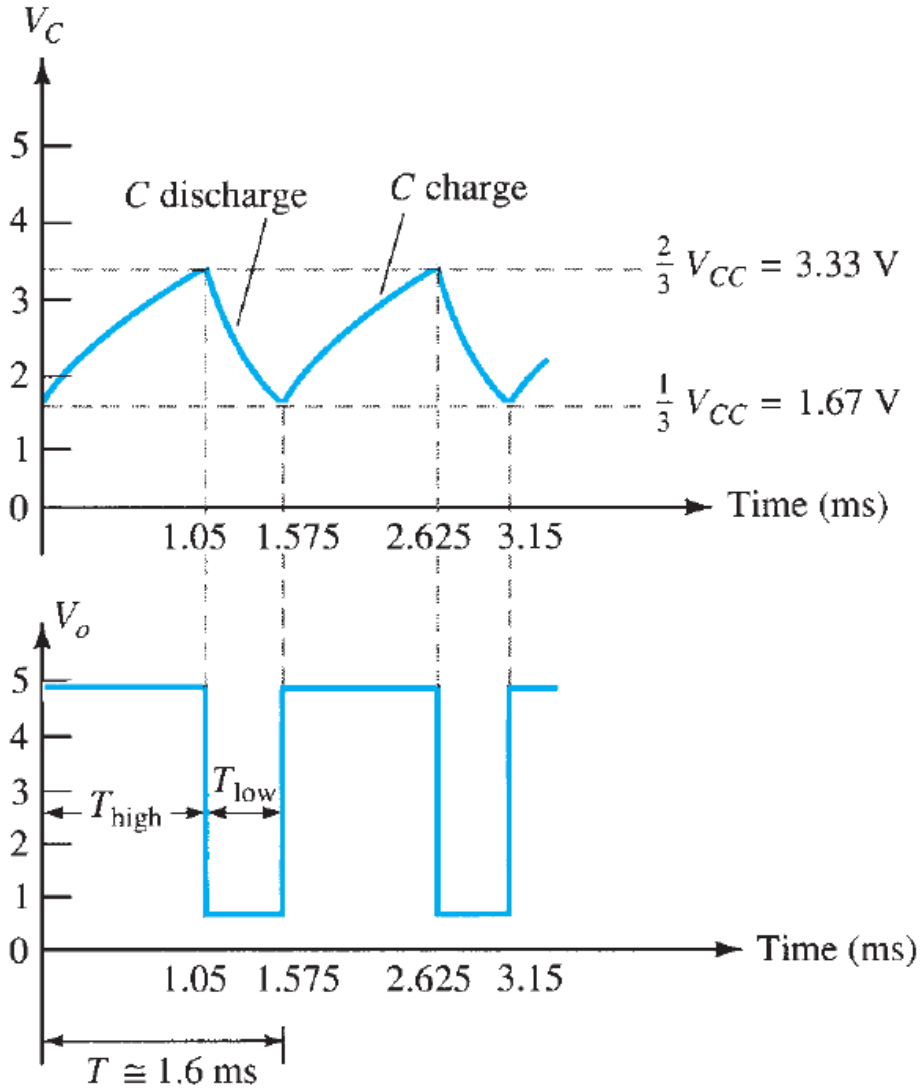


$$T_{high} \approx 0.7(R_A + R_B)C$$

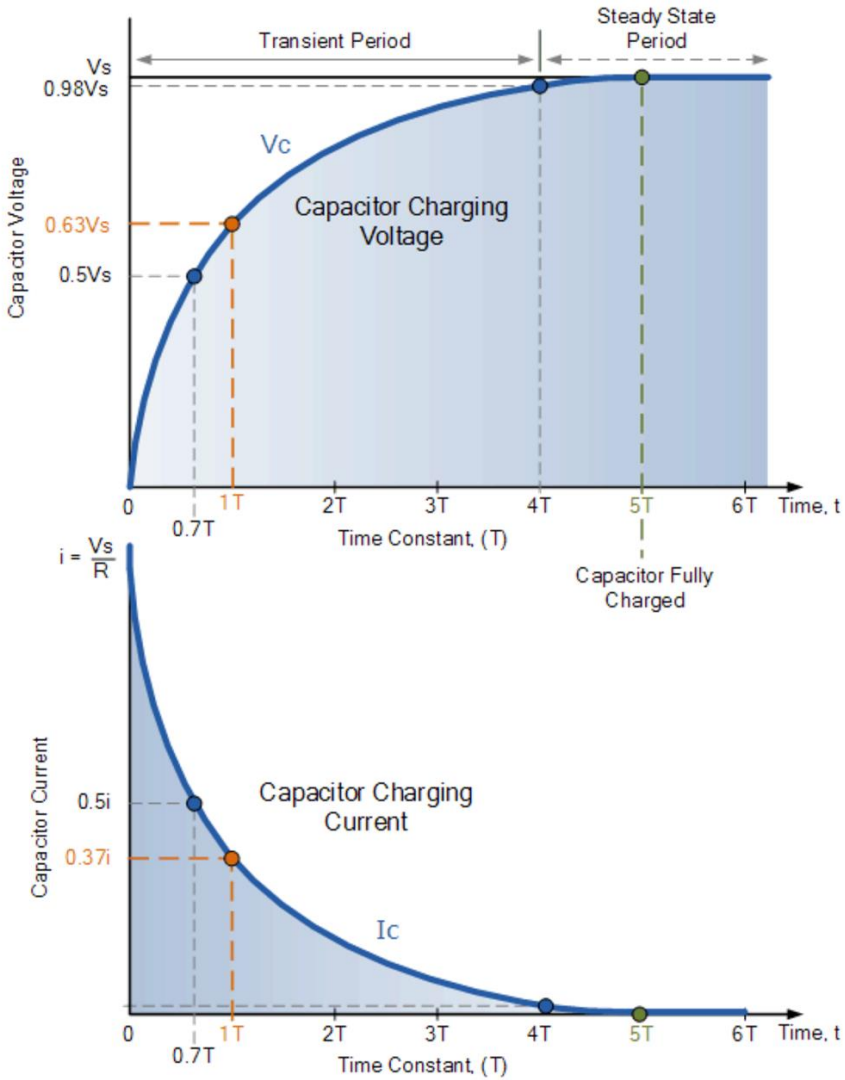
$$T_{low} \approx 0.7R_BC$$

$$T = \text{period} = T_{high} + T_{low}$$

$$f = \frac{1}{T} \approx \frac{1.44}{(R_A + 2R_B)C}$$



Timer IC Unit Operation



$$T_{\text{high}} \approx 0.7(R_A + R_B)C$$

$$T_{\text{low}} \approx 0.7R_BC$$

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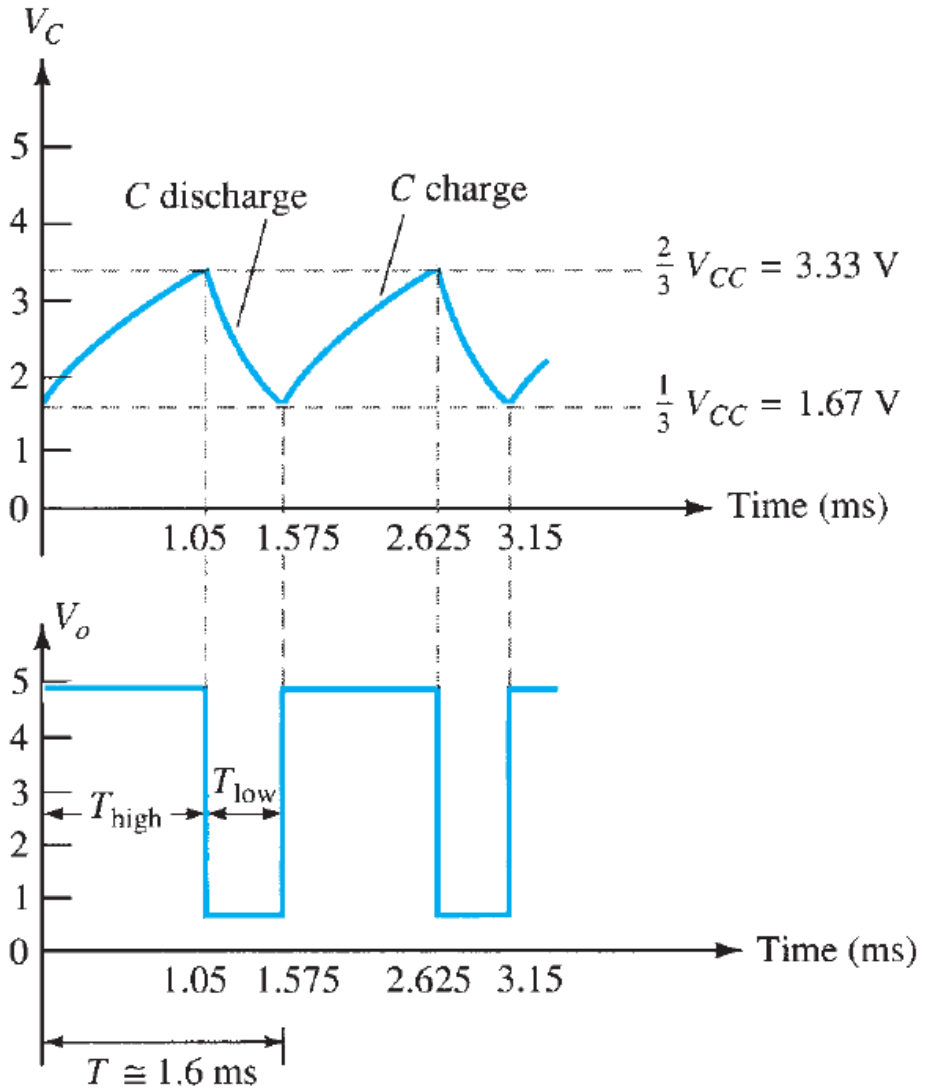
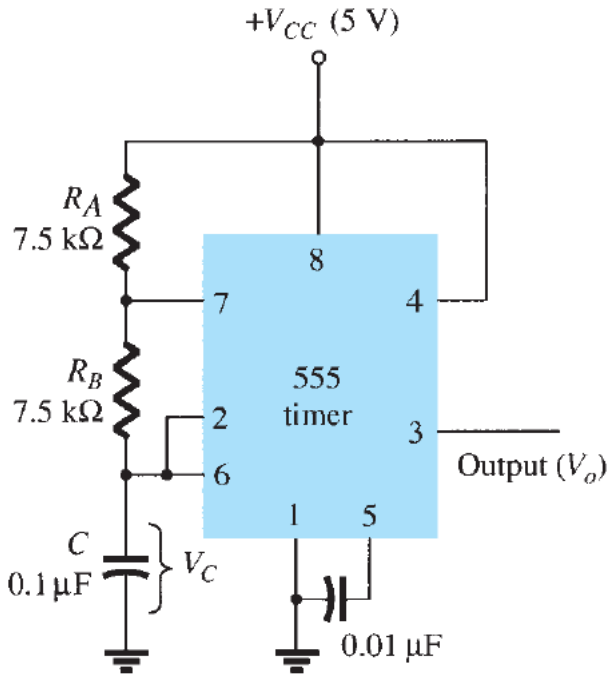


Timer IC Unit Operation



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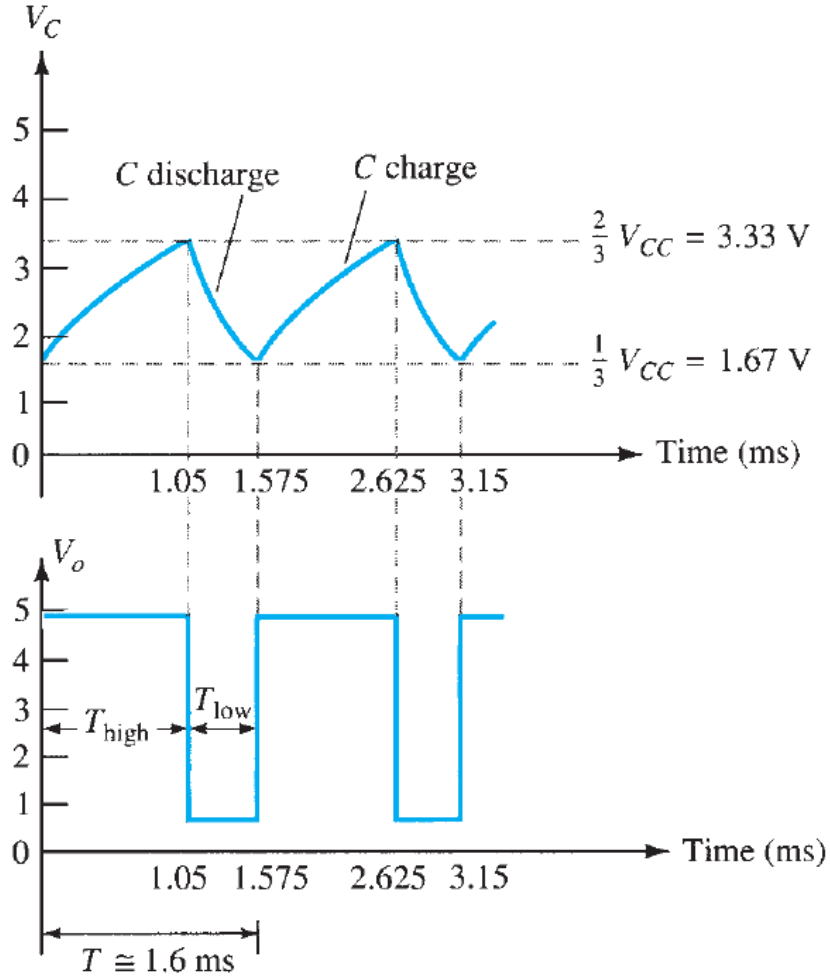


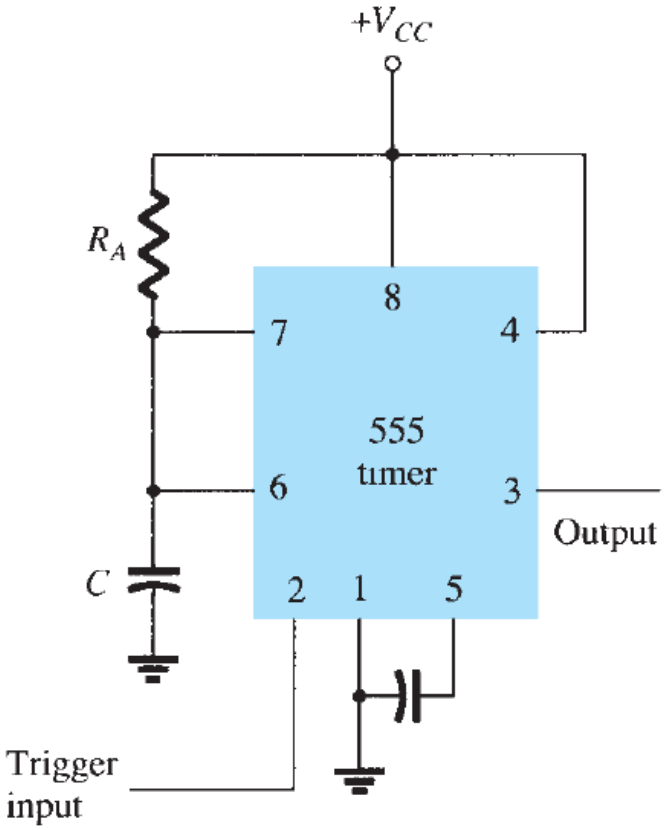
$$T_{\text{high}} = 0.7(R_A + R_B)C = 0.7(7.5 \times 10^3 + 7.5 \times 10^3)(0.1 \times 10^{-6})$$
$$= 1.05 \text{ ms}$$

$$T_{\text{low}} = 0.7R_BC = 0.7(7.5 \times 10^3)(0.1 \times 10^{-6}) = 0.525 \text{ ms}$$

$$T = T_{\text{high}} + T_{\text{low}} = 1.05 \text{ ms} + 0.525 \text{ ms} = 1.575 \text{ ms}$$

$$f = \frac{1}{T} = \frac{1}{1.575 \times 10^{-3}} \approx \mathbf{635\ Hz}$$

Timer IC Unit Operation



- When trigger input signal goes negative, it triggers the one-shot, with output at pin 3 then going high for a time period given by

$$T_{high} = 1.1R_AC$$

- Negative edge of the trigger input causes comparator 2 to trigger the flip-flop, with the output at pin 3 going high
- Capacitor C charges toward V_{CC} through resistor R_A
- When the voltage across the capacitor reaches the threshold level of $2V_{CC}/3$, comparator 1 triggers the flip-flop, with output going low
- The discharge transistor also goes low, causing the capacitor to remain near 0V until triggered again